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Design and Implementation of High-Speed Electronics for a Spatial Filter Velocimeter

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Acronyms

BGA	Ball Grid Array
CBA	Cost Benefit Analysis
CONSENS	CONceptual design Specification technique for the ENgineering of complex Systems
DSP	Digital Signal Processor
EMC	Electromagnetic Compliance
EMI	Electromagnetic Interference
FFT	Fast Fourier Transform
FPGA	Field-Programmable Gate Array
LVDS	Low-voltage differential signaling
McASP	Multichannel Audio Serial Port
PCB	Printed Circiut Board
PDN	Power Distribution Network
PLC	Programmable Logic Controller
SFV	Spatial Filtering Velocimeter
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
VADER	Velocimeter using ADvanced spatial filtER

1 Introduction

The aim of this thesis is the development of a custom hardware prototype used for the advancement of the spatial filtering algorithm. The derivation of the overall system requirements and the system design phase are carried out according to the CONceptual design Specification technique for the ENgineering of complex Systems (CONSENS) method, created by the Heinz Nixdorf Institut in Paderborn [1].
This project is conducted at the Institute of Systems engineering at the Bochum University of Applied Sciences in cooperation with Smart Mechatronics GmbH. The agreed project scope is attached to the data-cd (Appendix A.1.1).

A typical measuring task in an industrial environment is the determination of the velocity and length of produced material, such as wire. This task is often fulfilled by rotary encoders, or similar contact based instruments. However some surfaces prohibit the usage of contact based sensors, requiring non contact measurement [2].

Two concurring techniques for non contact measurement are established: the Laser-Doppler-Velocimetry (LDV) and the Spatial Frequency Velocimetry (SFV) [3]. The Institute of Systems engineering focuses on the research of improving spatial frequency algorithms. The introduction to the spatial filtering algorithm is only briefly described in this thesis, for a detailed explanation refer to the literature [3, 4, 5, 6].

Figure 1.1 shows the principal working of the spatial filter, showing a single particle moving perpendicular to an optical grid located in front of a camera. Light is reflected from the surface of the measured object and is projected onto the optical grid.

The resulting radiated power generates the spatial filter function $g(t)$, shown in figure 1.1 as a sinusoidal function. With the optical grid properties and the known cameras frame rate, the spatial filter function can be analysed regarding the frequency components which correlate to the measured velocity v of the object.

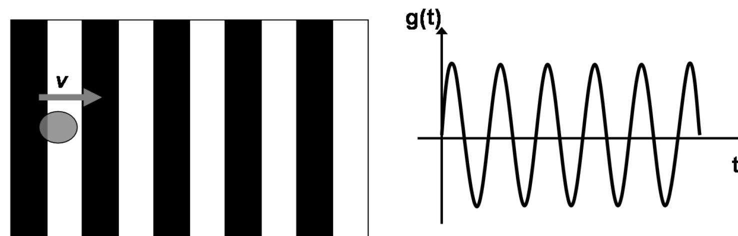


Figure 1.1: Spatial filter signal of a single particle [3]

As the project is carried out according to the v-model, the structure of the thesis is arranged similarly, describing the overall system requirement, the system design, the implementation and the verification in chronological order [7].

2 Foundations/Theory

This chapter gives a brief introduction into the principles and theoretical foundations utilised for the thesis. The main focus lies on techniques and principles utilised to describe and analyse systems consisting of high speed digital signaling.

2.1 LVDS

Low-voltage differential signaling (LVDS) defines a unidirectional data transmission standard for high speed data transfer. The physical layer is standardised by ANSI/TIA/EIA-644 as well as by IEEE, without defining the application layers to ensure usability for multiple purposes [8, 9].

The schematic circuit structure of a typical LVDS interface is shown in figure 2.1. The driver consists of a current source and two pairs of switches, limiting the output current per channel to 3.5 mA, resulting in an odd mode signal. The receiving end is terminated with a resistor of matching impedance to the transmission line, that produces the differential voltage signal for the receiver. The signal currents are limited to the wire pair resulting in a minimised loop area. This reduces coupling mechanisms and results in an improved noise immunity compared to single ended signaling.
In addition, the driver current limitation allows for hot plugging and also prevents spike currents occurring during level transitions, allowing data rates of up to 3.25 $\mathrm{Gbit\,s^{-1}}$ per channel [8].

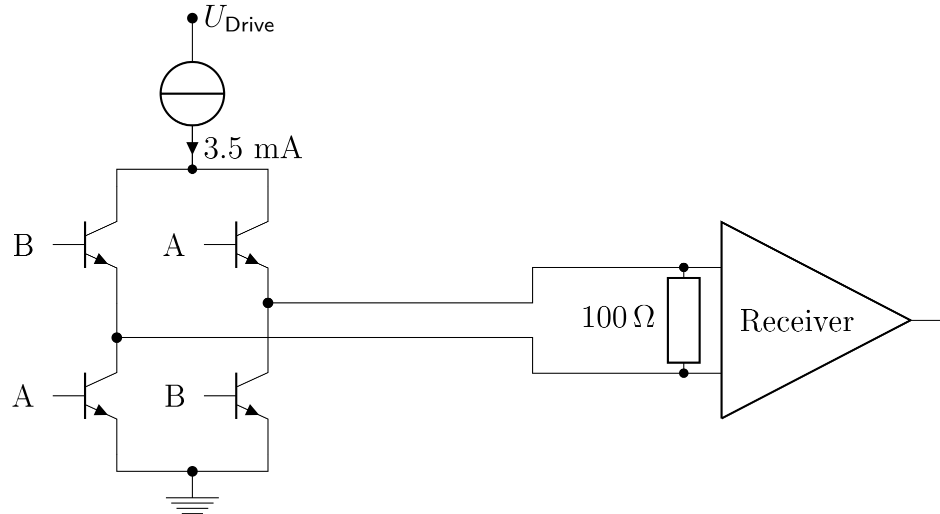


Figure 2.1: Schematic circuit structure of LVDS physical layer

Due to the minimised voltage swings, typically 300 mV, low slew rates of less than 1 V ns^{-1} can be achieved, which is considered as non critical for Electromagnetic Interference (EMI) [8]. Typical LVDS-receivers tolerate up to ±1 V ground shift, leading to a common mode range of 0.3 V to 2.3 V [10, 11].

2.2 Decoupling

In the supply of digital systems, current transients occur due to switching logic components. To minimise resulting voltage ripples, bypass capacitors are placed next to switching components. To estimate the necessary amount and type of decoupling, the capacitors impedance has to be modelled as a function of capacity, frequency, package type and mounting style to estimate the resulting ripple voltages caused by current transients. Therefore an equivalent circuit according to figure 2.2 is introduced. It consists of the ideal capacity C, the parasitic inductance L_{ESL} and the resistance R_{ESR}. To account for leakage currents, the parallel resistance R_{LEAK} is typically modelled, but is ignored for the decoupling analysis, as its influence is mainly limited to static behaviour.

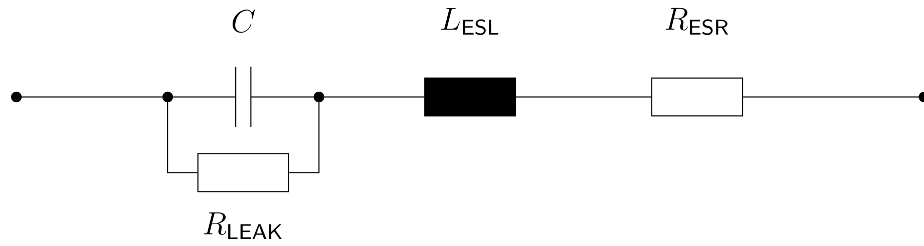


Figure 2.2: Equivalent circuit of a real capacitor

According to the equivalent circuit, the magnitude of the equivalent impedance can be calculate using equation 2.1.

$$|Z(\omega, R_{\mathsf{ESR}}, L_{\mathsf{ESL}}, C)| = \sqrt{R_{\mathsf{ESR}}^2 + \left(\omega L_{\mathsf{ESL}} - \frac{1}{\omega C}\right)^2} \tag{2.1}$$

To visualise the impact of different casing dimensions and therefore package impedances, two capacitors in different casings and with different capacitance are simulated and compared. Firstly a 100 nF capacitor in a 0402 package, with an inductance of 840 pH and an R_{ESR} of 0.2 Ω is simulated. Secondly a 1 µF capacitor in a 1206 casing, with a parasitic inductance of 1.2 nH and an R_{ESR} of 0.3 Ω is analysed. [12]

Both impedances are plotted in figure 2.3, as well as the resulting impedance of both capacitors in parallel configuration. The behaviour is mainly influenced by the change in capacitance, but also the change in inductance influences the resulting impedance.

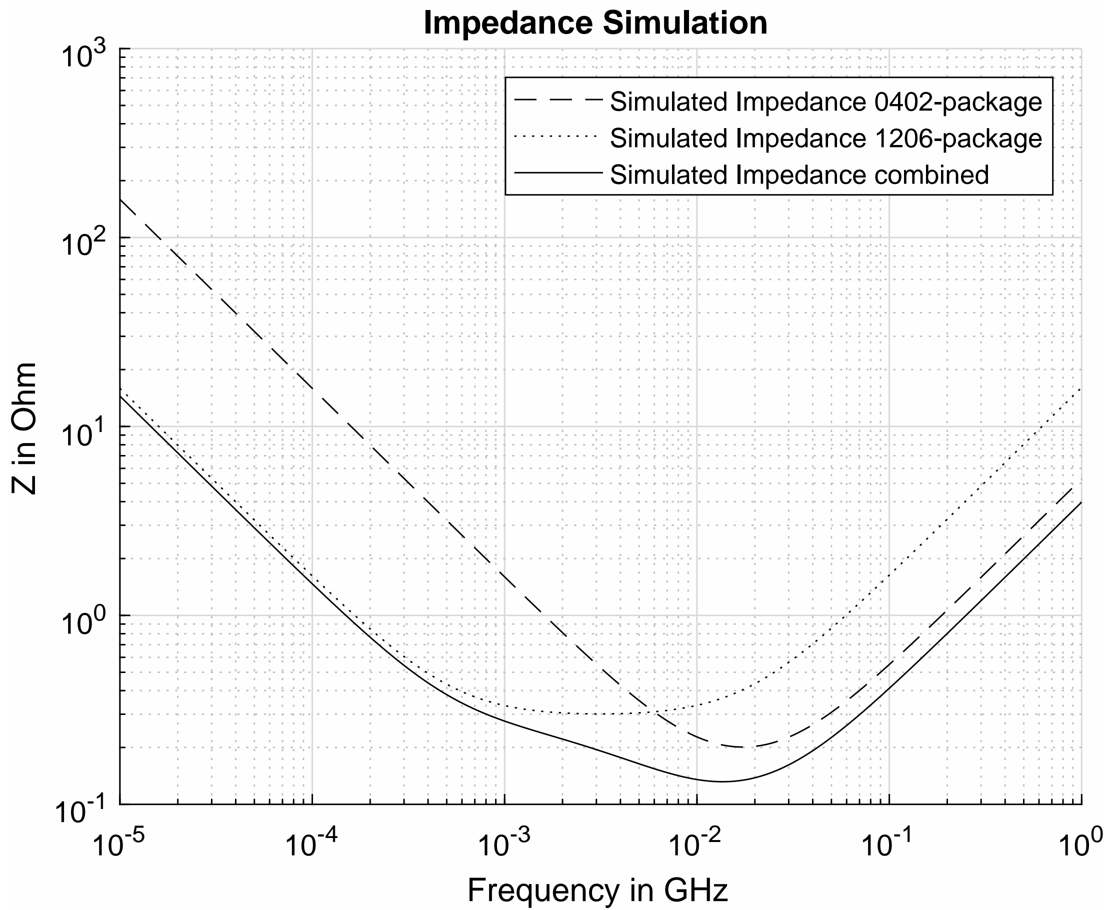


Figure 2.3: Simulated Impedances of 0402 and 1206 Ceramic Capacitors

The simulation does not include the estimation for the inductances caused by vias, connecting the capacitors to the actual power plane. To estimate this inductance, the geometry according to figure 2.4 for two spaced vias of equal diameter needs to be analysed analysed.

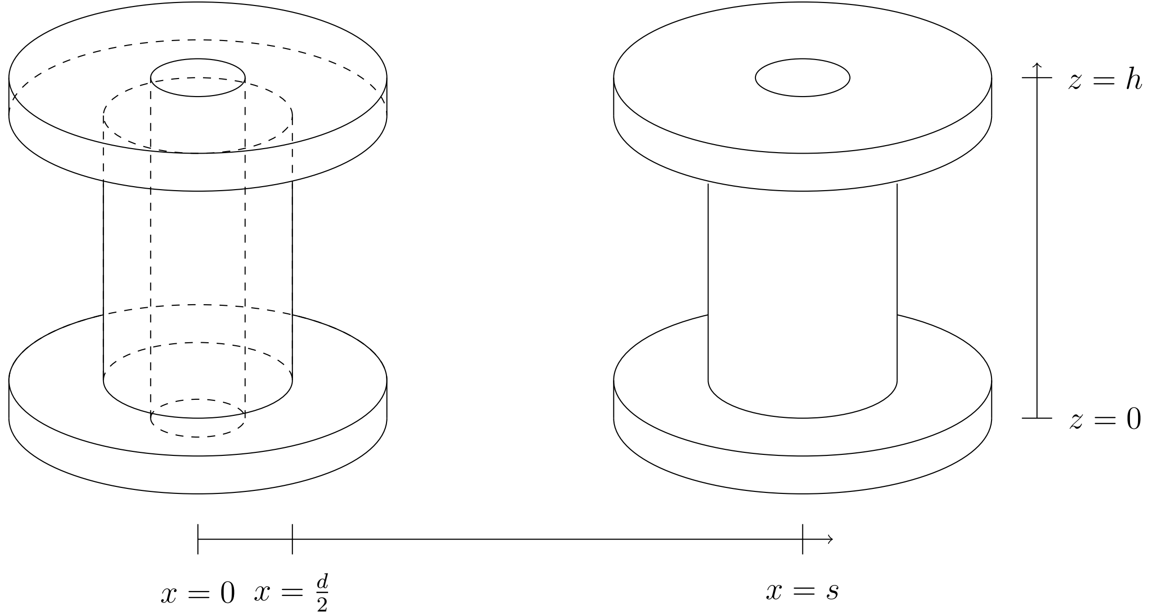


Figure 2.4: Inductance estimation of spaced vias

The magnetic field B between the vias is approximated by the following equation as a function of the distance x to the radius $d/2$ of the via.

$$B = \frac{\mu \cdot I}{2\pi x} \qquad x \geq d/2$$

In The defining formula of inductance, the magnetic flux Φ can be substituted as the surface integral of the magnetic field B. The surface integral is defined as the spanned area between the vias. Equation 2.2 yields the formulated geometry-dependant estimation of the vias.

$$L_{\mathsf{Via}} = \frac{\Phi}{I} = \frac{2}{I} \int B \mathsf{dA} = \frac{2}{I} \int_0^h \int_{\frac{d}{2}}^{s-\frac{d}{2}} \frac{\mu I}{2\pi x} \mathsf{dxdz} = \frac{\mu}{\pi} \cdot h \cdot \ln\left(\frac{2s}{d} - 1\right) \tag{2.2}$$

With this inductance estimation as well as the parasitic properties taken from data sheets, the quality of the proposed decoupling array can be estimated [13].

2.3 Transmission Line

As signaling speed increases the properties of electrical circuitries can no longer be accounted for as purely resistive but rather estimated as segments containing parasitic impedances. As these properties are described in great detail in the literature such as Heuermann in [14], only a brief introduction is given here.
The electrical properties of a conductor section Δz can be modelled according to figure 2.5 by a serial inductance to model the generated magnetic field , a capacitor to account for generated electrical fields and an admittance to account for the isolation resistance.

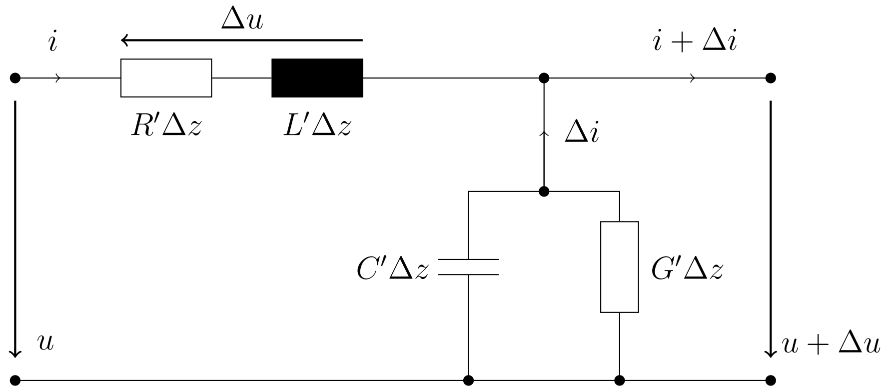


Figure 2.5: Schematic transmission line characteristics for a conductor section Δz, [14]

Applying Kirchhoff's laws and rearranging them to equal Δi and Δu yields the following equations:

$$\Delta i = -G'\Delta z \cdot (u + \Delta u) - C'\Delta z \cdot \frac{\mathrm{d}(u + \Delta u)}{\mathrm{d}t} \quad \text{and} \quad \Delta u = -R'\Delta z \cdot i - L'\Delta z \cdot \frac{\mathrm{d}i}{\mathrm{d}t}$$

As the limit of Δz approaches 0, the two equations yield a differential change in voltage and current:

$$\frac{\partial i}{\partial z} = -G'u - C'\frac{\partial u}{\partial t} \quad \text{and} \quad \frac{\partial u}{\partial z} = -R'u - L'\frac{\partial i}{\partial t} \tag{2.3}$$

These differential equations can easily be solved for the case of sinusoidal steady-state, using the following phasors:

$$\underline{U} = \frac{\hat{u}}{\sqrt{2}} \cdot e^{j(\omega t + \phi_\mathrm{u})} \quad \text{and} \quad \underline{I} = \frac{\hat{i}}{\sqrt{2}} \cdot e^{j(\omega t + \phi_\mathrm{i})} \tag{2.4}$$

Inserting these phasors into equations 2.3 and applying the rules of derivation results in:

$$\frac{\partial \underline{I}}{\partial z} = -(G' + \mathrm{j}\omega C')\underline{U} \quad \text{and} \quad \frac{\partial \underline{U}}{\partial z} = -(R' + \mathrm{j}\omega L')\underline{I}$$

Combining both first order differential equations into a single second order differential equation results in:

$$\frac{\partial^2 \underline{U}}{\partial z^2} - (R' + \mathrm{j}\omega L')(G' + \mathrm{j}\omega C')\underline{\mathrm{U}} = \frac{\partial^2 \underline{U}}{\partial z^2} - \underline{\gamma}^2 \underline{\mathrm{U}} = 0 \tag{2.5}$$

The propagation constant $\underline{\gamma}$ comprises the real part attenuation constant α and the imaginary part β.

$$\underline{\gamma} := \sqrt{(R'G' - \omega^2 L'C') + \mathrm{j}\omega(R'C' + L'G'))} = \alpha + \mathrm{j}\beta$$

Solving equation 2.5 a generalised solution consists of the initial conditions $\underline{U}_{\mathrm{r0}}$ and $\underline{U}_{\mathrm{v0}}$ with a first and third quadrant solution of the complex root, that represent the incident voltage $\underline{U}_{\mathrm{v}}$ and the reflected voltage $\underline{U}_{\mathrm{r}}$ as functions of z.

$$\underline{U}(z) = \underline{U}_{\mathrm{r0}} \cdot e^{\underline{\gamma} z} + \underline{U}_{\mathrm{v0}} \cdot e^{-\underline{\gamma} z} = \underline{U}_{\mathrm{r}} + \underline{U}_{\mathrm{v}} \tag{2.6}$$

To find an equation for the impedance of a conductor segment, equation 2.3 is utilise to find a substitution for $\underline{I}$ as a function of $\underline{U}$, which yields:

$$\underline{I} = -\frac{1}{R' + \mathrm{j}\omega L'} \cdot \frac{\partial \underline{U}}{\partial z} = -\frac{\underline{\gamma}}{R' + \mathrm{j}\omega L'} \underline{U}(z) \tag{2.7}$$

Using Ohm's law, this results in the familiar equation for the impedance of a conductor segment, equation. 2.8:

$$\underline{Z}_0 = \frac{R' + \mathrm{j}\omega L'}{\underline{\gamma}} = \sqrt{\frac{R' + \mathrm{j}\omega L'}{G' + \mathrm{j}\omega C'}} \tag{2.8}$$

For the pre-layout trace impedance calculation, estimative equations 2.9 and 2.10, proposed by Johnson in [13] are used.

In addition to the estimation by the above formulae, a numerical solver (Saturn PCB) is used to verify the plausibility of the results.

$$Z_{0(Microstrip)} = \frac{60}{\sqrt{0.475\ \epsilon_R + 0.67}}\ \ln\left(\frac{4h}{0.67 \cdot (0.8w + t)}\right) \tag{2.9}$$

$$Z_{0(Stripline)} = \frac{60}{\epsilon_R}\ \ln\left(\frac{4b}{0.67\pi \cdot (0.8w + t)}\right) \tag{2.10}$$

The physical dimensions for the formulae 2.9 and 2.10 are depicted in figure 2.6

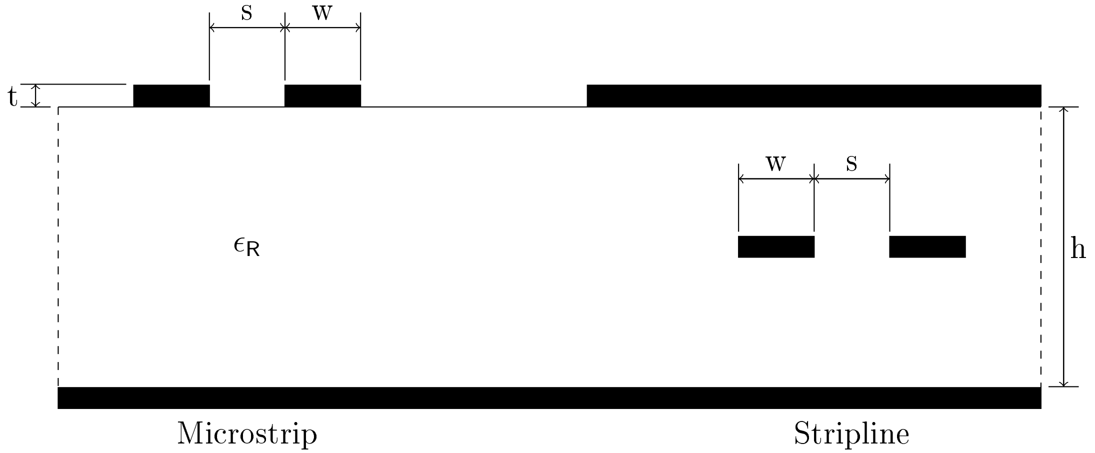


Figure 2.6: Transmission Line Geometry [15, 16]

2.3.1 S-Parameters

As shown in the calculation of transmission lines, voltages and currents in transmission lines are highly dependant on the location of measurement. For high frequency signals, it is therefore convenient to describe networks in terms of waves [14]. The incident waves a_i are defined as incident voltage U_p wave, normalised over the root of the reference impedance $\sqrt{Z_{Li}}$, figure 2.7, while the reflected wave b_i is the reflected voltage U_r normalized to $\sqrt{Z_{Li}}$.

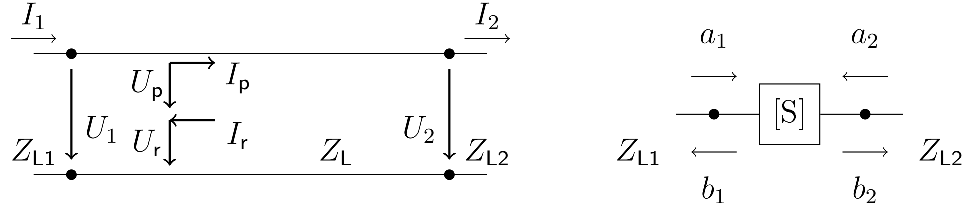


Figure 2.7: Transformation of 4-pole network with currents and voltages to 2-port wave network

If the internal impedance of the network differs from the reference impedance, the definition for a_i and b_i are given as equation 2.11:

$$a_\mathrm{i} = \frac{\underline{U}_\mathrm{i} + Z_\mathrm{Li} \cdot I_\mathrm{i}}{2\sqrt{\mathrm{Re}\left(Z_\mathrm{Li}\right)}} \quad \text{and} \quad b_\mathrm{i} = \frac{\underline{U}_\mathrm{i} - Z_\mathrm{Li} \cdot I_\mathrm{i}}{2\sqrt{\mathrm{Re}\left(Z_\mathrm{Li}\right)}} \tag{2.11}$$

The relationship of a_i and b_i can then be written as a linear equation system, as equation 2.12 depicts for a 2-port network, with the coefficient matrix referred to as the scattering matrix:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.12}$$

The matrix coefficients can be briefly described as:

S_{11}: Input port reflection coefficient

S_{12}: Reverse transmission coefficient

S_{21}: Forward transmission coefficient

S_{22}: Output port reflection coefficient

The parameters S_{11} and S_{22} can be described as reflection coefficients for matched loads. The parameter S_{21} defines the forward transmission coefficient and the parameter S_{12} the reverse transmission coefficient. To qualify networks in regard to their attenuation and reflection, distortion return losses R_L and insertion losses I_L are often used, calculated as follows, equation 2.13.

$$R_\mathrm{L} = 20\ \log\left(\frac{1}{|S_\mathrm{ii}|}\right) \quad \text{and} \quad I_\mathrm{L} = 20\ \log\left(\frac{1}{|S_\mathrm{ij}|}\right) \tag{2.13}$$

Typically conductors are considered good for less than 3 dB attenuation and no more than -10 dB reflection [14].

2.3.2 Signal Delay

To determine the propagation speed of a signal through a transmission line, equation 2.6 can be used under the assumption that after time Δt at Δz the phase of the signal is the same as at $t = 0$ and $z = 0$.

$$\underline{U}_{\mathsf{v}}(\Delta z) = \underline{U}_{\mathsf{v0}} \cdot e^{-\alpha \Delta z} \tag{2.14}$$

For a sinusoidal voltage this leads to the following equation:

$$U_{\mathsf{v0}} \cdot e^{-\alpha \Delta z} \cdot \cos(\omega \Delta t + \phi_{\mathsf{v}} - \beta \Delta z) = U_{\mathsf{v0}} \cdot \cos(\phi_{\mathsf{v}}) \cdot e^{-\alpha \Delta z} \tag{2.15}$$

For the equation to be true, the cosine argument must equal zero, meaning that $\omega \Delta t$ must also equal $\beta \Delta z$. Solving for the deviation of distance over time produces the definition of the propagation speed v_{ph}:

$$v_{\mathsf{ph}} = \frac{\Delta z}{\Delta t} = \frac{\omega}{\beta} \tag{2.16}$$

For approximated lossless conductors, assuming $\beta \approx \omega \cdot \sqrt{L'C'}$, the propagation speed can be estimated as follows:

$$v_{\mathsf{ph}} = \frac{\omega}{\beta} = \frac{\omega}{\omega \cdot \sqrt{L'C'}} = \frac{1}{\sqrt{L'C'}}$$

To match trace length in the implementation, it is efficient to think of propagation speed as the propagation delay per length. Johnson [13] gives the following delay estimations for PCB traces as function of the dielectric constant:

$$T_{\mathsf{D}}(Microstrip) = 33.36\ \sqrt{0.475\ \epsilon_{\mathsf{R}} + 0.67}\ \frac{\mathrm{ps}}{\mathrm{cm}} \tag{2.17}$$

$$T_{\mathsf{D}}(Stripline) = 33.36\ \sqrt{\epsilon_{\mathsf{R}}}\ \frac{\mathrm{ps}}{\mathrm{cm}} \tag{2.18}$$

2.3.3 Skew

As signal speed increases, the timing constraints between data setup time and sampling time decrease. This increases the impact of timing imperfections, such as skew induced by driver circuit switching time variations or unbalanced trace lengths.
To ensure that valid data is present at the receiver during the data sampling window, fig. 2.8, a worst-case jitter estimation based on the given specifications from the receiver data sheet is mandatory.

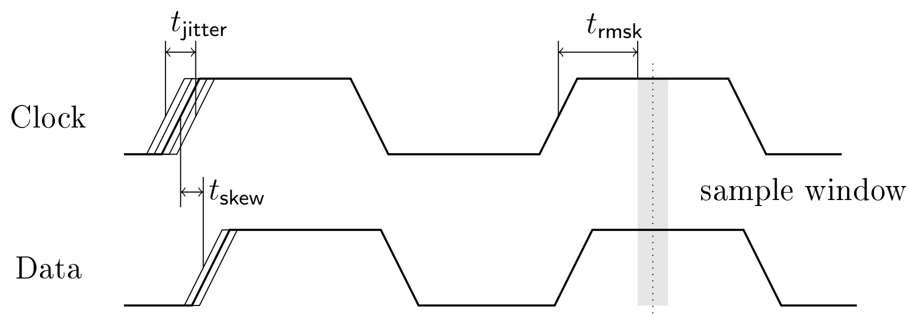


Figure 2.8: Example timing diagram, showing jitter and skew

Adding up the available skews, such as the transmitter jitter and the jitter induced by cables, then subtracting these from the receiver sampling time t_{rmsk}, an estimation of remaining skew for the Printed Circiut Board (PCB) traces t_{skewPCB} can be derived, eq. 2.19:

$$t_{\mathsf{skewPCB}} = t_{\mathsf{rsmk}} - t_{\mathsf{jitter}} - t_{\mathsf{skewCable}} \tag{2.19}$$

Using the propagation delay formulae, the maximum trace length derivation for a given interface can be calculated.
In addition to the timing imperfections, effects such as crosstalk, impedance differences in traces or electromagnetic noise in general influence the signal quality. A common tool to measure the overall signal quality is the eye-diagram.

2.4 Eye-diagrams

The data eye diagram is a technique to qualify high speed data signals. It shows multiple important characteristics of the signal so that its quality can be determined.
It is constructed by laying individual bits of a high speed signal into a single graph, with signal amplitude as the vertical axis and time as the horizontal axis. The resulting graph is a statistical representation of the high speed signal. [17]

The characterising elements of the measurement are shown in figure 2.9. The rise time t_{rise} and fall time t_{fall} are defined as the average transition duration from one logical state to another, measured from 10 % to 90 % level of the slope. The eye width is defined as the time between two mean crossing from one logical state to another. The eye height defines the minimal voltage between the two logical states within the diagram. It determines the eye closure caused by noise and thereby how well the logic states can be distinguished from another. The crossing percentage represents the mean height of the level transition and is an indicator for asymmetry in bit durations. Jitter is defined as the derivation of the actual timing of transitions to the ideal transition eg. caused by clock skew or pulse width distortion. It can be random or deterministic depending on the source of the interference.

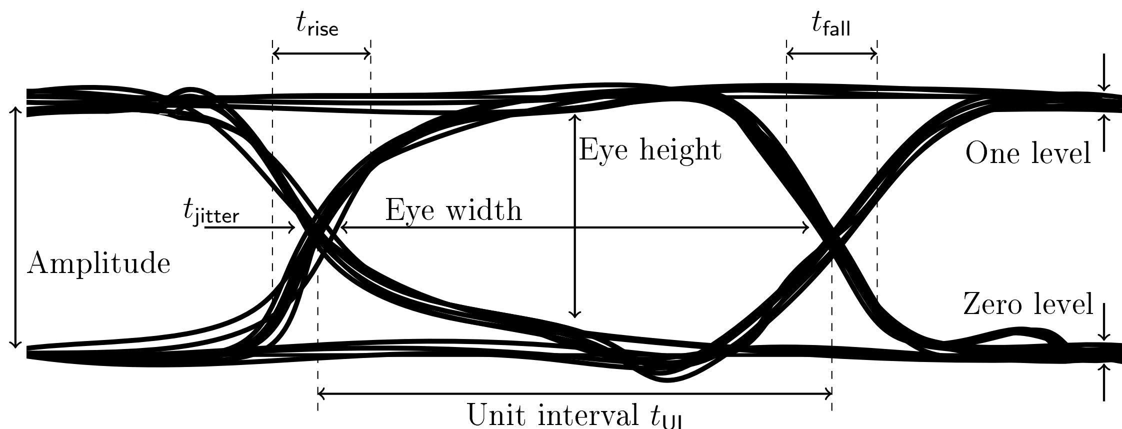


Figure 2.9: Typical eye-diagram [17]

3 Requirements

According to the CONSENS method, the first step during the requirements engineering is the definition of an environment-model. It allows for an overview of all influencing environmental elements linked to the system [1].
The specific environment-model for the Velocimeter using ADvanced spatial filtER (VADER) is shown in figure 3.1. It is evaluated in collaboration with the all involved project parties to aim for completeness of linked elements. The requirements document is then derived from the environment-model (see Appendix A.1.2).

Describing the specific environmental elements, A key element is the surface area of the measured object. It interacts with the VADER-system via the optics and the camera.
The length measurement interface and the incremental encoder describe two industry standard interfaces, commonly used for rotary encoders. As VADER is intended to replace these in existing processes, the usage of the quadratic incremental encoder and the Synchronous Serial Interface (SSI) are predetermined by the customer. Furthermore VADER has to be able to identify process borders, instigated by material entering the cameras scanned area, to implement the length measurement. As a result of this, photo electric sensor interfaces are necessary, as they are used in industrial processes to indicate the start or end of a process.

The industrial environment necessitated requirements regarding ambient temperature, dust concentration, humidity, power supply quality and Electromagnetic Compliance (EMC). Specific standards that the VADER system has to comply with are stated in the requirements document, Appendix A.1.2.

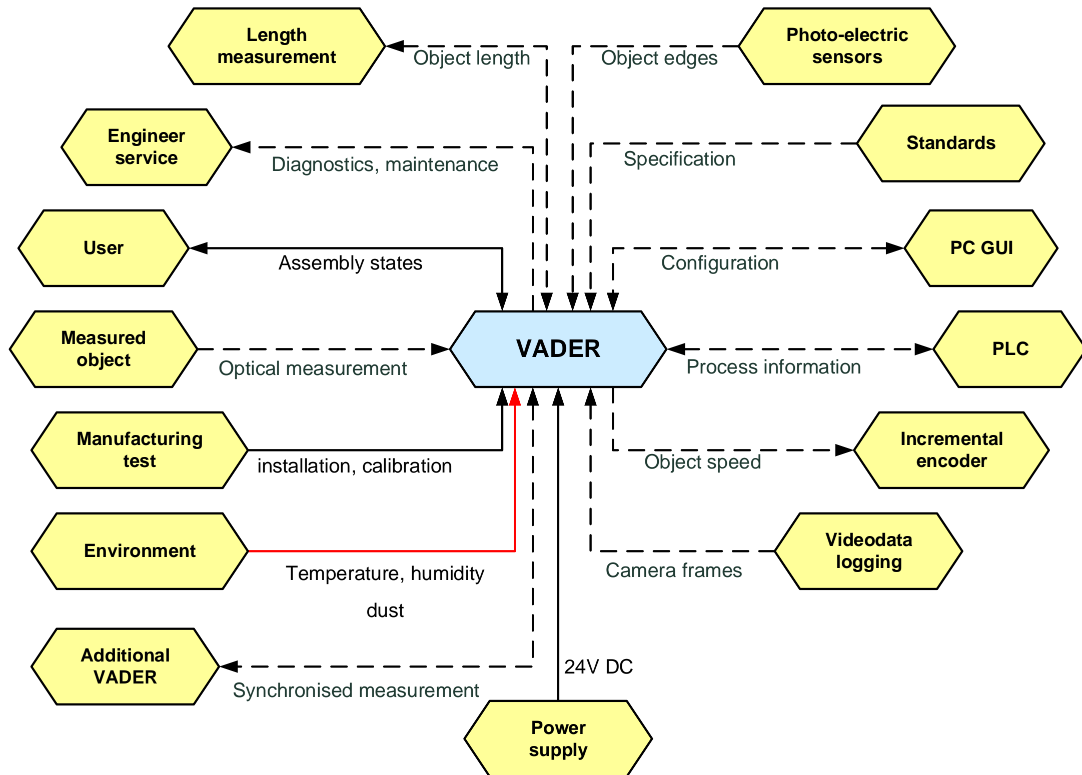


Figure 3.1: Derived environment-model for the VADER-system

To be able to set the correct filtering values for every application, it is necessary to store the raw optical data of the process for later analysis. For this purpose a logging system with the capability of storing raw process data with durations of up to 20 min is required.

For communication with a host in a given production environment such as a Programmable Logic Controller (PLC), VADER must be equipped with a universal field bus interface, to allow for easy implementation of an interface to a predetermined communication protocol.
The configuration of the system by a service engineer as well as the readout of parameters and debugging of the software requires a specific communication interface. Furthermore status LEDs visible during the normal operation of VADER in the process are required, to indicate the state of operation to the user.

4 System Design

With the overall system requirements determined, a suiting system architecture is derived, as shown in Fig. 4.1. The electronics system element consists of the necessary circuitry to communicate with all interfacing elements and hosts the hardware purposed for the computing of the spatial filter algorithm. External connections through the casing are depicted within the diagram as hexagons on the casing boundary, representing a connector that has to comply with the environmental requirements.

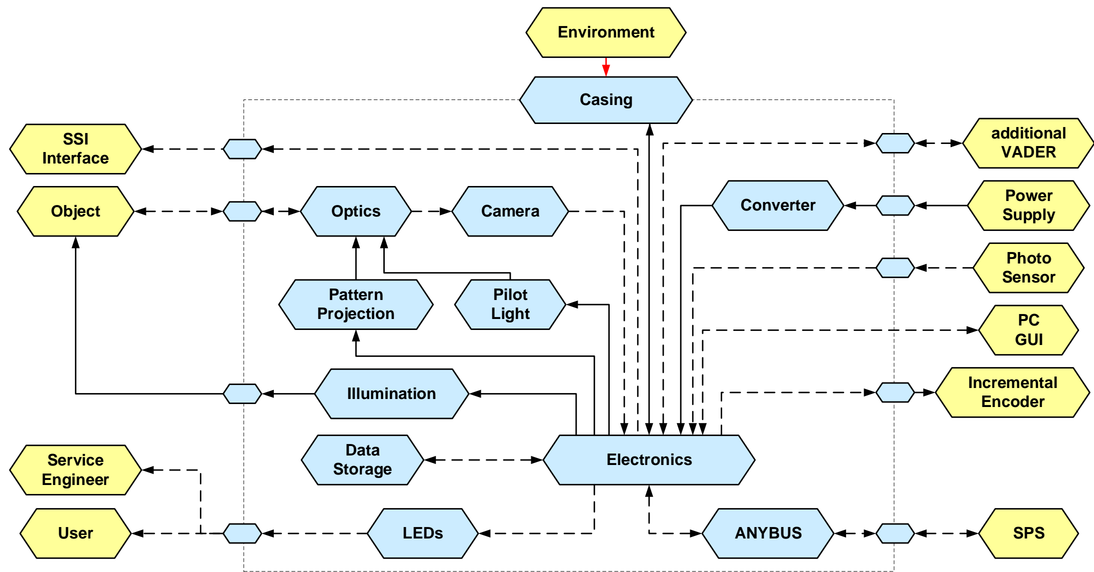


Figure 4.1: Proposed system architecture VADER

Explanation of the system elements:

- Camera: Implementing the spatial filter algorithm with a camera is set by project specifications.

- Optics: Optical system mounted to camera, the elaboration of a suitable solution is not part of this thesis.
- Pattern Projection and Pilot Light: Future extensions to the optical system, are not part of this thesis.
- Illumination: Light source to illuminate the measured objects structural features.
- Data Storage: Device to store raw video images as specified in the requirements.
- LEDs: External indication for users.
- ANYBUS: Universal field bus interface to ensure versatility.
- Converter: External voltage converter and filter.
- Casing: Mechanical enclosure housing all system elements and protection from environmental influences.

To minimise the utilised PCB area, an external voltage converter for the 24 V external supply to a 12 V level is chosen, which also handles the EMC filtering. Furthermore the outsourcing of the converter minimises the design risks of the hardware development.
As solution for the required universal field bus interface, the Anybus M40 module system is chosen, which consists of a standardised PCB connector and offers a variety of field bus implementations [18].
External LEDs are added to meet the requirements of externally visible state indicators for both the user and service-engineer.
The data storage device is housed within the casing of the VADER system, as the necessity of raw image data extractions only arises during the initial setup of the sensor in a given environment.
Due to the requirements regarding the maximum camera data rate and the implementation of the spatial filtering algorithm, the usage of a FPGA alongside a dedicated Digital Signal Processor (DSP) is the chosen system architecture [3].

The spatial filter function, consisting of large vector multiplication and addition is optimally performed by programmable logic, whereas the Fast Fourier Transform (FFT) and auto correlation functions are best performed by a DSP. The selection of suitable devices for these tasks is described in the course of this chapter.

Figure 4.2 shows the intended data flow of the resulting Spatial Filtering Velocimeter (SFV)-sensor, in which the raw images are transferred from the camera to the FPGA via a high speed interface. The interface also allows for configurations to be sent from the FPGA to the camera, which is further described in section 4.4.
The FPGA applies the spatial filter function to the raw images, transfers camera parameters controlled by the DSP, such as the exposure time to the camera and handles the communication to external interfaces.
The resulting spatial filter function is transferred to the DSP for the spatial analysis, yielding the velocity and length measurement results.
These results are transferred back from the DSP to the FPGA, which in turn broadcasts it via the specific external interfaces. The external interfaces also contain the data storage interface, allowing for raw image data storage.
A detailed description of the implemented algorithm is given by Schneider in [19].

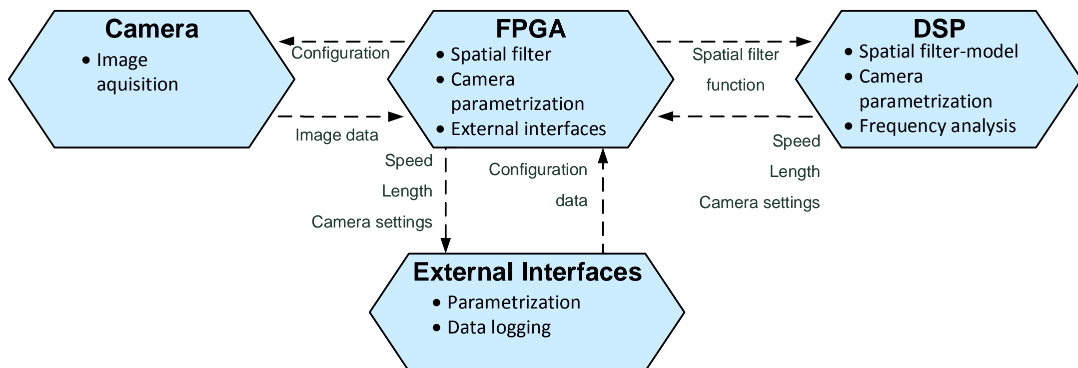


Figure 4.2: Block diagram of information flow of the spatial filter velocimeter [3]

4.1 FPGA selection

To decide upon the best suiting FPGA for the VADER project, multiple model architectures are taken into account. As the project team already has experience with the equipment and software offered by Xilinx, other vendors are not taken into further consideration. To illustrate the selection process, two competing device series are compared:

- The Xilinx Spartan 6 series is widely used and offers a verity of available development-boards. It includes dedicated serial transceivers supporting data rates of up to 3.2 $\mathrm{Gbit\,s^{-1}}$ and can be used with DDR2 and DDR3 RAM [20].
- The Xilinx 7 family comprises of the Artix-7 series, which are purposed for low power applications with high logic throughput. They consist of 6.2 $\mathrm{Gbit\,s^{-1}}$ GTP-transceivers, supporting the SATA 6 $\mathrm{Gbit\,s^{-1}}$ standard. Furthermore the DDR3 and DDR3L standard are supported as RAM interfaces. [21, 22]

Table 4.1 depicts a Cost Benefit Analysis (CBA), comparing two specific devices from each series, the Artix-7 XC7A35T and the Spartan 6 XC6SLX45T, meeting the requirement for the estimated number of IO pins. The key characteristics are the available DSP slices needed to perform multiplications, the transceivers maximum data rate purposed for the raw image storage as well as the experience of the project team with the given family.

Table 4.1: CBA to elicit suiting FPGA series for the VADER project

		XC7A35T		XC6SLX45T	
Criterion	%	val.	%	val.	%
GTP-Transceiver	17.3%	1.8	15.6%	1.0	8.7%
Logic Cells	13.3%	1.2	8.0%	1.2	8.0%
DSP Slices	20.0%	1.3	13.0%	1.0	10.0%
Embedded RAM	18.7%	1.0	9.3%	1.3	12.1%
Price	11.3%	1.3	7.4%	1.1	6.2%
Experience	19.3%	1.5	14.5%	1.2	11.6%
Result			67.8%		58.6%

As the CBA in table 4.1 shows, the Artix-7 series FPGA is the best suited architecture, as the availability of the hight speed transceivers as well as the larger amount of DSP slices are beneficial for the VADER project.

4.2 DSP selection

To evaluate the best match for the data processing, information on the latest DSPs from TI is gathered. In the domain of high performance processing, TI offers the C66x Core, which runs on a maximum of 1.25 GHz clock frequency and is declared as high performance fixed and floating point DSP [23]. For the computation tasks the VADER project possesses, a single core suffices to perform the DSP tasks, as the spatial filtering algorithm has little potential for parallel executions [3].
TI uses its KeyStone Multicore Architecture to integrate multiple cores into one package, leading to two main groups of processors, the TMS320x series and the 66AK2x series. The TMS320x series compose of up to 8 C66x cores with dedicated coprocessors for specific tasks, such as Ethernet. The 66AK2x combines a C66x core with an Arm Cortex-A15 Microprocessor, allowing to address a wide variety of peripherals.

Two specific devices are compared, that fulfil the DSP requirements for the VADER project, the TMS320C6655 DSP and the 66AK2G12 System-on-Chip.
The TMS320C6655 consists of one C66x core, a selection of peripherals such as SPI, Ethernet and PCIe, and characterises as power efficient solution for DSP tasks.
The 66AK2Gx processor consists of a C66x core alongside an A15 ARM core, offering a variety of peripherals, including 30 IO pins, USB 3.0 support, 3 Serial Peripheral Interface (SPI) interfaces as well as a dedicated Ethernet coprocessor. Table 4.2 shows the CBA used to decide upon the most suiting DSP. As some of the system elements are connected directly to the DSP, the availability of peripherals and GPIO pins is an important factor for the decision. Furthermore the availability, the programming complexity and the availability of development boards influence the decision.

Table 4.2: CBA comparing the TMS320C6655 to the 66AK2G12 [23, 24]

		66AK2G12		TMS320C6655	
Criterion	%	val.	%	val.	%
Peripherals	15.4%	1.6	12.3%	0.9	6.9%
Availability	9.3%	1.0	4.6%	1.3	6.0%
GPIOs	13.2%	1.5	9.9%	1.0	6.6%
Programming complexity	11.4%	0.9	5.1%	1.3	7.4%
SIMULINK support	17.1%	1.0	8.6%	1.0	8.6%
Price	10.7%	1.0	5.4%	1.2	6.4%
Maximal clock rate	10.4%	1.0	5.2%	1.0	5.2%
Development board	12.5%	1.5	9.4%	1.2	7.5%
Result			60.5%		54.7%

As table 4.2 shows, the 66AK2Gx Processor is the better suited option, as it comprises more specific peripherals, supports a larger number of dedicated GPIO pins and offers a better support of development boards, even though it is not yet as broadly available as the TMS320C6655.

4.3 Data storage Interface

To select the interface between the data storage and the VADER system, the following requirements have to be taken into account:

1. Minimum raw-image capture duration: 20 min
2. Maximum data rate of camera interface
3. Data storage system removable

The maximum data rate of the camera interface f_{Data} derives from the requirements of a maximum camera frame rate $f_{\mathsf{Framerate}}$ of 200 kHz, and the number of pixels per frame N_{Pixel} of 1024 using 12 bit per pixel, equation 4.1.

$$f_{\mathsf{Data}} = N_{\mathsf{BitsPerPixel}} \cdot N_{\mathsf{Pixel}} \cdot f_{\mathsf{Framerate}} = 410\ \mathrm{MB\,s^{-1}} \quad (4.1)$$

Taking into consideration the storage duration of 20 min and the camera data rate, a minimum storage capacity of 492 GB is needed.

Table 4.3 lists a selection of commonly used high speed interfaces, that support a removable data storage system. It lists the maximum supported write speed as well as the main advantages and disadvantages.

Table 4.3: Data storage interface benchmark

Interface	**max. Storage**	**max. write speed**	**Pro**	**Con**
SDXC	2 TB	25 $\mathrm{MB\,s^{-1}}$	easy assembly	doesn't meet speed requirements
USB 2.0	1 TB	60 $\mathrm{MB\,s^{-1}}$	common interface	power and data over same connector
USB 3.0 (Gen1)	1 TB	500 $\mathrm{MB\,s^{-1}}$	high writing speed	power and data over same connector
SATA 3 $\mathrm{Gbit\,s^{-1}}$	30 TB	300 $\mathrm{MB\,s^{-1}}$	FPGA IP support	higher power requirements
SATA 6 $\mathrm{Gbit\,s^{-1}}$	30 TB	600 $\mathrm{MB\,s^{-1}}$	FPGA IP support	higher power requirements

The SDXC interface consists a serial interface, composed of four data lines and a designated clock. The voltage levels of 3.3 V allow easy implementation in embedded systems however limit the achievable data rate [25].
The USB 2.0 standard consists of a 200 mV differential link, via which the bidirectional communication between master and slave is handled. This leads to an achievable data rate of 60 $\mathrm{MB\,s^{-1}}$, not meeting the writing speed requirements.
The USB 3.0 interface includes 4 additional LVDS pairs in addition to the standard differential link, allowing for a maximum data transfer speed of 900 $\mathrm{MB\,s^{-1}}$ [26].
Both SATA interfaces consist of two data lanes each appointed to transmitting or receiving. It is supported by IP-Cores within the Vivado IDE, and the SATA 6 $\mathrm{Gbit\,s^{-1}}$ is backward compatible to the 3 $\mathrm{Gbit\,s^{-1}}$ standard. The key advantage of the SATA interface towards the USB 3.0 standard is the separation of power supply and data transfer into two separate cables, making the integration of connectors less critical.
Therefore the SATA interface is chosen as interface between VADER and the data storage device.

4.4 Camera Interface

For the decision upon a suitable camera interface, high speed line scan cameras from different vendors are evaluated. The most common interfaces for these are Camera Link and Gigabit Ethernet (GigE Vision), however cameras with Thunder Wire and USB 3.1 interfaces are also available [27, 28, 29].
Table 4.4 lists the proposed interfaces with the maximum achievable data rate, the number of cables as well as the proposed cable lengths and the connector type.

Table 4.4: Camera Interface Benchmark [30, 29]

Digital System Interface	**Data Transfer Rate**	**Cable Length**	**Connector**	**# Cables**
GigE Vision	125 $\mathrm{MB\,s^{-1}}$	100 m	RJ45	1
Camera Link Base	255 $\mathrm{MB\,s^{-1}}$	10 m	26Pin	1
Camera Link Medium	510 $\mathrm{MB\,s^{-1}}$	10 m	26Pin	2
Camera Link Full	680 $\mathrm{MB\,s^{-1}}$	10 m	26Pin	2
USB 3.1	900 $\mathrm{MB\,s^{-1}}$	3 m	USB type 3	1

The necessary transfer rate of 410 $\mathrm{MB\,s^{-1}}$ limits the selection to Camera Link Full, Camera Link Medium and USB 3.1.
As USB 3.1 is a recent standard, not many cameras are supported at the time of the project [27, 28], therefore the decision to use Camera Link Medium as link between FPGA and camera is made.

The Camera Link standard cable consists of four data LVDS pairs, a clock pair for the data lines, four control pairs for a general camera control interface as well as two pairs reserved for an asynchronous serial communication link. This cable can be used for the Camera Link base connection [30]. The second cable, used additionally for the Camera Link medium standard, contains two additional data ports, each consisting of one clock and four data LVDS pairs. Figure 4.3 shows the cable configuration according to the Camera Link standard [30].

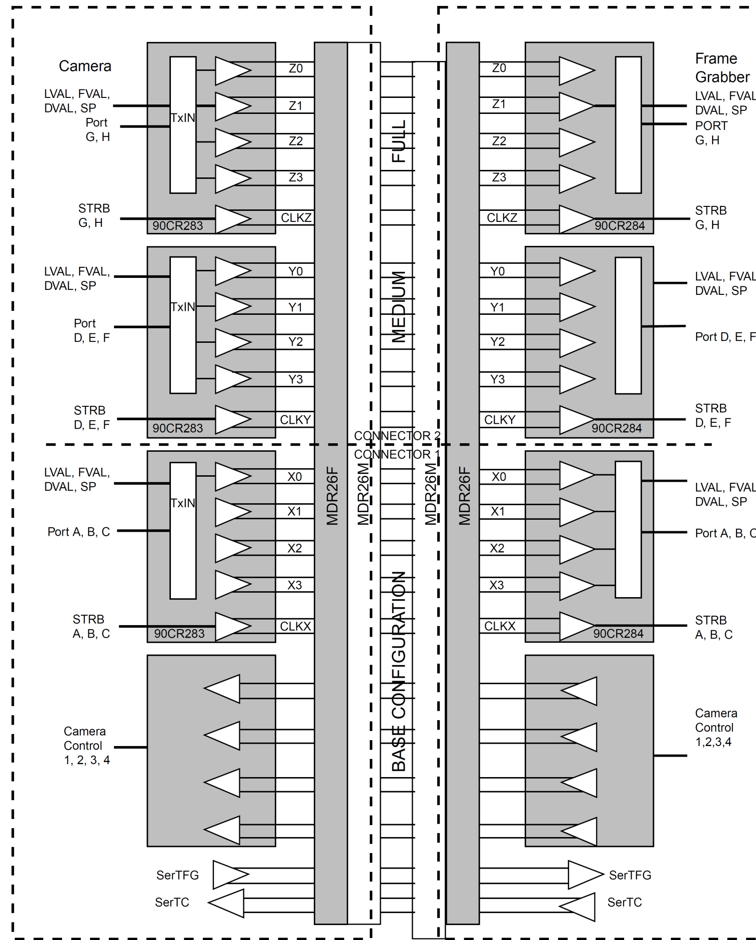


Figure 4.3: Camera Link cable configuration according to standard [30]

The Camera Link standard [30] recommends the usage of TIs DS90CR287 Channel Link receivers, which converts the four LVDS channels into 28 parallel data signals of TTL levels. Even though the chosen Artix-7 FPGA consist of pin pairs supporting the LVDS standard, it is decided to use the dedicated channel link chips, so that the FPGA is not directly connected to a connector.

4.5 System Architecture

With the selected solutions for the critical system elements in place, the detailed system architecture can be produced.

In order to minimise the design risk, a split system architecture is proposed, which separates the electronics system element at the link between the DSP and the FPGA. As the DSP is intended primarily to fulfil the computational effort and the FPGA is supposed to handle external interfaces, the decision is made to develop the FPGA related hardware in the course of this project and use one of the already available DSP development boards. This ensures a functioning prototype as a result of this thesis, and a platform to optimise the spatial filter algorithms.

The EVMK2GX development, shown in Fig. 4.4, is chosen for the prototype, as it comprises suitable peripherals for communication such as multiple SPI, Ethernet and a Multichannel Audio Serial Port (McASP) interfaces. To ensure that all necessary communication between DSP and FPGA, specified in Appendix A.1.2 can be handled by the selected bus, the McASP interface is chosen, as the EVMK2GX board has enough channels connected to an external header to achieve the estimated necessary data rate of 10 $\mathrm{MB\,s^{-1}}$. [31]

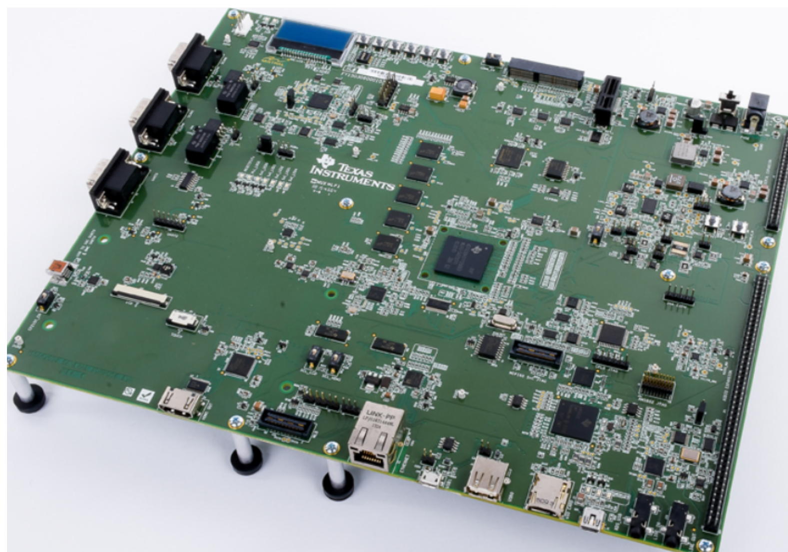


Figure 4.4: Chosen 66AK2Gx DSP development board from TI

The chosen development board determines the first system element for the FPGA board, as the McASP interface is connected to an external pin header, which is used as a physical link between development board and the custom hardware.

The data storage system is also designed onto the custom electronics, with an additional RAM storage device connected to the FPGA to act as data buffer for the storage interface.
The external interfaces for photo sensors, incremental encoders, ANYBUS and SSI are also part of the custom electronics.
Taking these considerations into account, a system architecture, referred to as the FPGA board, according to figure 4.5 is derived.

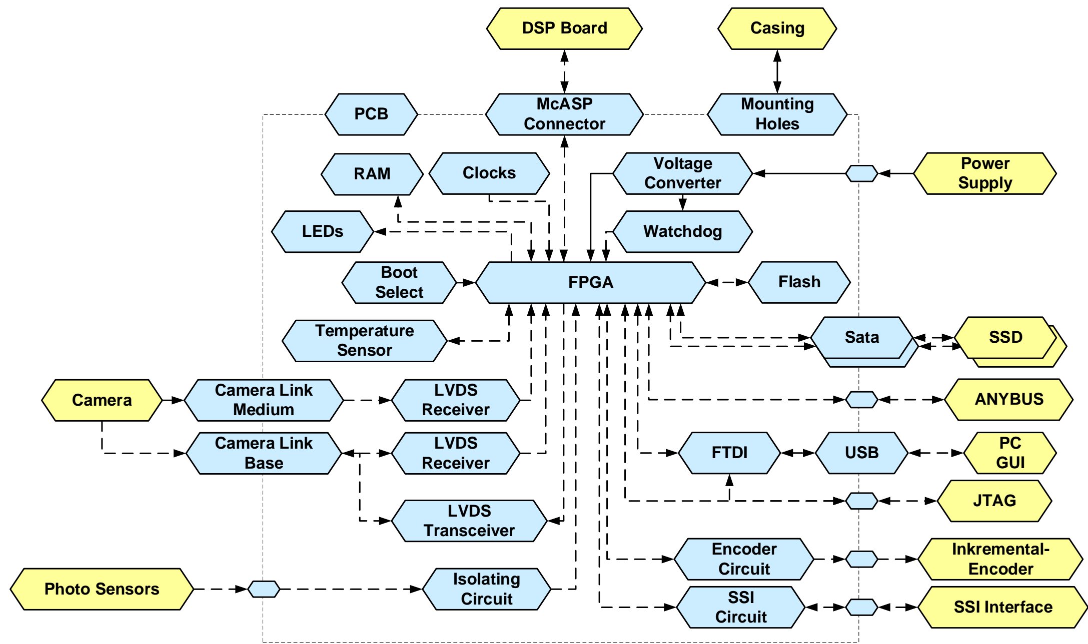


Figure 4.5: Proposed system architecture of the FPGA board

As the proposed system architecture is agreed upon with the customer, the detailed elaboration and analysis of all system elements is performed in the implementation phase.

5 Implementation

Documenting the implementation phase is sequenced according to the determined milestones of the project, firstly describing the power supply design, followed by the derivation of the schematic elements and then the implementation of the actual hardware. Each milestone is subject to a review, which is held in cooperation with Smart Mechatronics.
The iterative work-flow for the PCB design begins with the pre-route calculations, the routing of the layout, simulation of the high speed circuits and optimisation of the layout, as described in chapter 6. The final step is the verification of the physical hardware, see chapter 7 [7].

5.1 Power Supply

The first step of the implementation phase is the evaluation of the power supply scheme starting with the analysis of all used components regarding their required supply voltage and corresponding supply current. Table 5.1 shows the accumulated currents for the main supply levels, the detailed calculation and the complete list of consumers is attached in Appendix A.1.6.
In addition to the worst-case currents the absolute minimum and maximum voltages for each level are recorded, to estimate the output voltage tolerances.
The generated power supply requirements document is attached in Appendix A.1.3.

Table 5.1: Current estimation for power supplies, detailed in Appendix A.1.6

Supply Rail	Output Current	Output Power
12.0 V	2.53 A	30.39 W
5.0 V	1.45 A	7.27 W
3.3 V	1.63 A	5.37 W
1.8 V	1.02 A	1.84 W
1.35 V	0.80 A	1.08 W
1.0 V	2.10 A	2.10 W

With the voltage margins and the estimated current consumption of the power rails, specific power supply solutions can be derived. Using the TI-WEBENCH as well as LTspice to confirm the correct dynamic behaviour, specific solutions according to figure 5.1 are chosen [32]. Each converter is subject to dimensioning calculation, worst-case estimation and thermal analysis, which are documented in Appendix A.1.6.

The LTC3636 dual-synchronous buck converter is used to provide the 1.0 V core voltage for the FPGA as well as the 3.3 V peripheral level, with a maximum output current of 6 A per channel. The start-up ramps can be adjusted separately for each channel and two power-good-outputs are available [33].
The voltages for the remaining auxiliary levels are provided by the three TPS82140 converters, which contain an integrated inductor, minimising the external component count. The maximum output current of 2 A is also sufficient for the selected voltage rails [34].
For the supply of the GTP-transceiver of the Artix-7 device two TPS7A7001 low-drop linear regulators are used. These allow for a calculated maximum voltage ripple per rail of 2 mV, thereby staying within the required voltage ripple of 10 mV [35, 36], Appendix A.1.3.

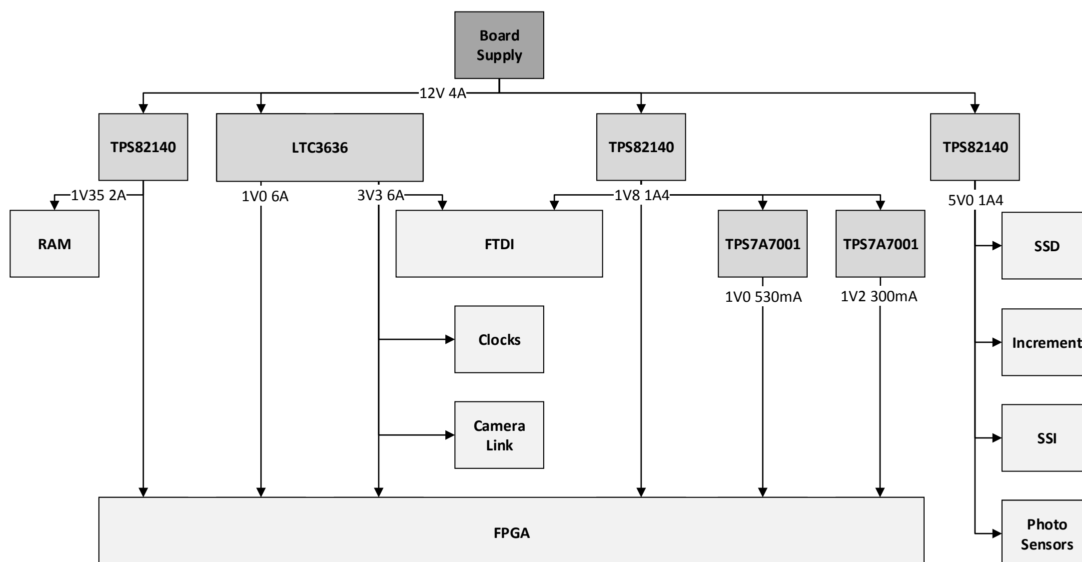


Figure 5.1: Implemented power-supply scheme

The voltage start-up sequence is primarily defined by the recommendation for the Artix-7 devices, described in [35], however the maximum slew rate of all voltage levels is verified for the remaining components on the PCB. Additionally Xilinx specifies the allowable maximum voltage between distinct rails during the start-up as 2.625 V to prevent increased current demand of the FPGA.
To comply with these requirements, there are two commonly used techniques to implement the start-up sequence, briefly described in the following: [37]

- Coincident: All voltages are ramped with constant slew rate, keeping voltage difference as small as possible, however increasing inrush currents as all decoupling capacitors get charged simultaneously.
- Sequential: voltage levels enabled after one another, leading to a reduction of supplying currents, however increasing differential voltages between different levels.

To balance the resulting inrush currents and differential voltages between rails, a combination of both start-up methods is chosen. The 1.0 V core rail and the auxiliary levels are started up coincidentally, while still reaching their target voltage in the recommended sequence as given by [35].

The 1.35 V supply is ramped with a reduced slew rate, to comply with the start-up recommendation of the chosen DDR3L chips data sheet specification [38]. Using this method, the maximum differential voltage of 2.625 V is never exceeded. As the recommended supply sequence for the GTP-transceiver is VCCINT, MGTAVCC, MGTAVTT, given by [35], the linear regulators are enabled in a sequential manner.

To ensure a deterministic start-up behaviour of the GTP-transceivers, the linear regulators for the MGTAVCC and MGTAVTT rails are enabled when both the 1.8 V and 5 V rail reach their specified operating voltage, by using the power-good-outputs to enable the linear regulators, figure 5.2.
The resulting start-up sequence of all implemented voltage levels and the RESET signal enabling the FPGA are depicted in figure 5.2.

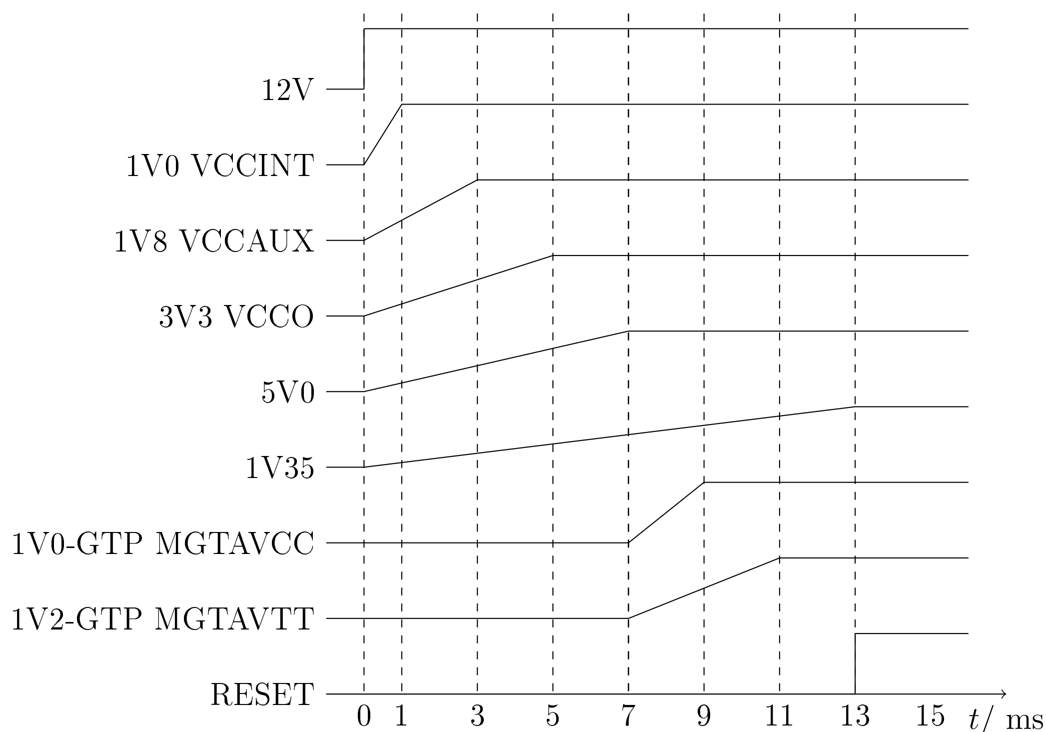


Figure 5.2: Power supply start-up timing diagram

5.2 Schematic

The schematic is created according to the system architecture, figure 4.5. Thereby all system elements are designed into hierarchical schematic sheets, allowing for traceability of all elements throughout the project. The description of the schematic derivation is done representatively for the key elements Camera Link base interface, power supply, DDR3 memory interface as well as the FPGA configuration and decoupling.
The completed schematic, cleared for implementation after the reviews is attached in Appendix A.3. The dimensioning and worst-case calculations are attached in Appendix A.1.7.

5.2.1 Power supply

The conception of the power supply schematic elements is documented for the LTC3636 dual buck converter, as the described steps transfer to all used converters. The implemented schematic section showing the LTC3636 and the connected external components is depicted in figure 5.3.

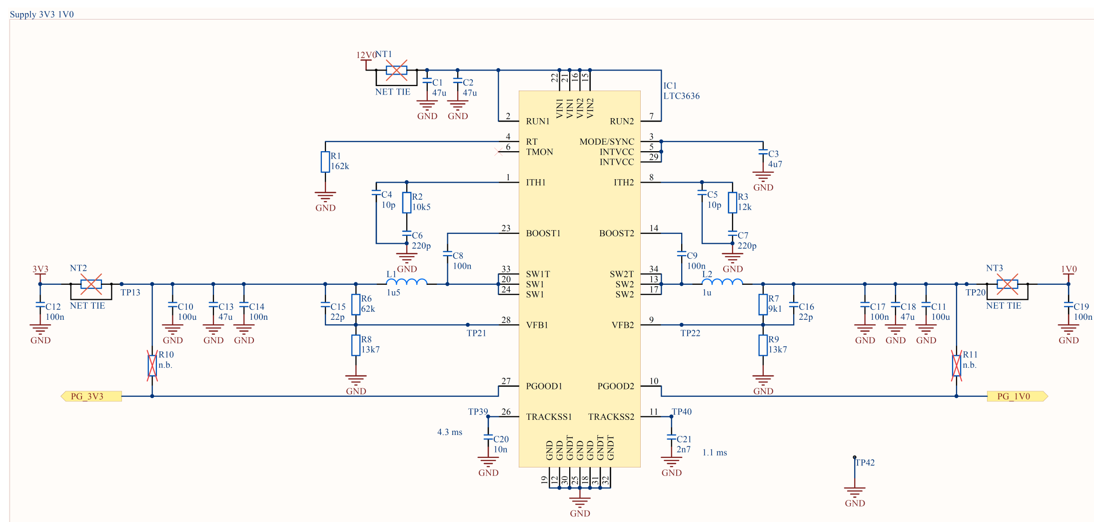


Figure 5.3: Schematic of the LTC3636 dual buck converter

The supply and output nets are connected via net ties, to allow the system to be isolated during the verification phase for testing.

Furthermore capacitors are placed close to the net ties connected to the outputs of the power supply elements, to set up a low pass filter if the output ripple requirements should not be met during the verification phase.
The power-good-outputs are connected to the reset circuit which generates the master-reset signal for the FPGA taking all voltage levels into account.

The worst-case calculation and component selection conducted for each power supply element is attached in Appendix A.1.6, as well as the simulation file used to verify the component behaviour for load transitions.

5.2.2 FPGA

The design of the FPGA schematic is a large part of the schematics milestone. The fist step is the configuration of the start-up boot circuitry. The FPGA can be configured to boot from a number of interfaces, however the selected boot options are JTAG and quad SPI. The JTAG is primarily intended to be used during debugging and testing, while the SPI interface is to be used during normal operation. Jumper J12 is connected to the FPGAs MODE2 pin and determines which interface is selected as boot option. The INIT_B-pin is connected to the reset signal which is generated by the power good circuit. In case a reset request has to be sent from the DSP, the RESET signal is also connected to one of the McASP signal pins via an optional resistor, to allow for the aforementioned option.

For debugging an LED is connected to the DONE_0 pin, which indicates the completed boot sequence. The resulting schematic section regarding the boot circuitry is shown in figure 5.4.

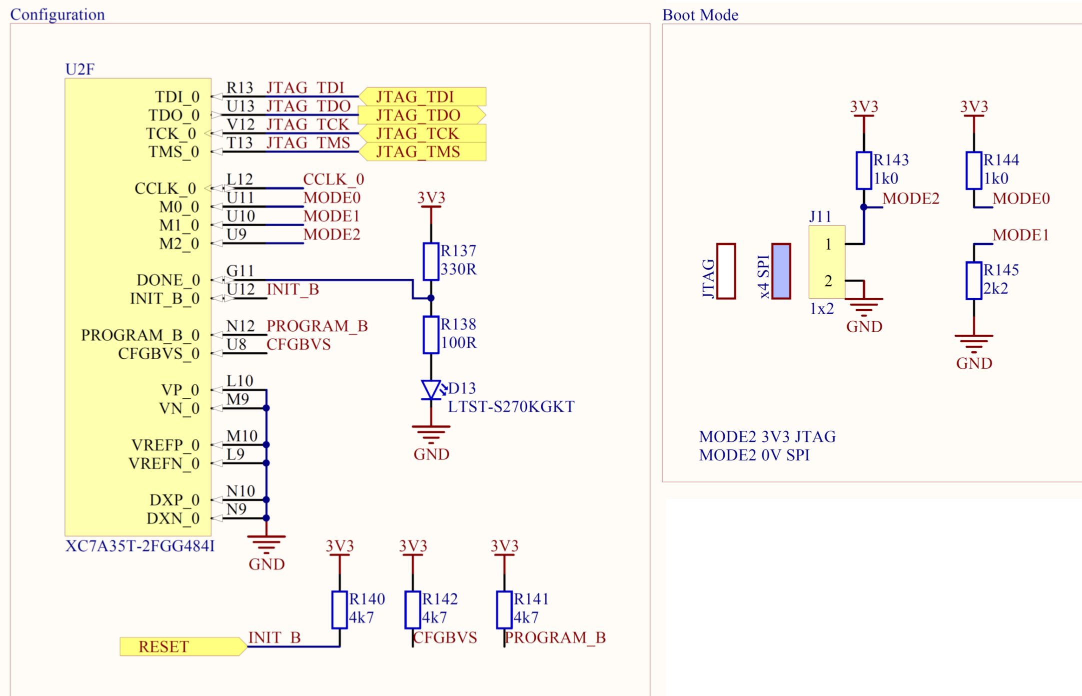


Figure 5.4: Schematic of the FPGA configuration circuit

To provide the system clock for the FPGA during debugging, an external 100 MHz oscillator is connected to bank 34 of the FPGA. The clock source for the main application can be chosen from either the camera pixel clock or the external oscillator.

The planning of the IO connection is done using a Vivado 18.0 pin-planning project, to minimise the risk of errors while connecting all schematic elements to the FPGA. To decide which elements are connected to which banks, the data flow within the FPGA as well as the planned PCB layout have to be taken into account, to minimise the length of the connecting traces. The documents created for this purpose are attached in Appendix A.1.15.

To optimise the effort of routing the low speed interface signal traces connected to the FPGA, the pin-swapping feature the Altium Designer offers is used, grouping all pins of a given bank into a pin-swapping group, allowing for optimised trace routing without trace crossings.

The initial configuration of the local decoupling network for the different power levels is implemented according to the Artix-7 PCB design guide [39].
It includes recommendations for specific capacitor values and packages for each of the used banks, and is intended to be used as a starting point. Figure 5.5 shows the placed decoupling capacitors for the core voltage VCCINT and the PLL-power supply VCCAUX. The simulation of the decoupling network as verification of adequate decoupling is described in the layout section 5.4.

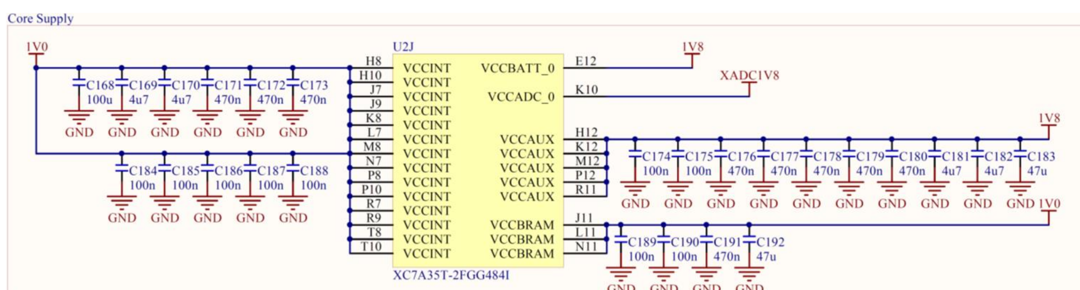


Figure 5.5: Schematic section decoupling capacitors FPGA VCCINT and VCCAUX

5.2.3 DDR3 Memory Interface

The selected DDR3 memory chip is the MT41K128M16JT-125 manufactured by Micron, supporting the DDR3LP standard, which reduces the logic voltage levels from 1.5 V to 1.35 V for better EMC [38]. It is supported by the memory interface generator (MIG-7) included in the Vivado 18 design suite and is used in the Digilent Arty development board [40].
The device is interfaced with a data bus width of 16 bit, and is addressed by a 14 bit wide address bus, allowing for a total 2 Gbit of volatile storage [38].

The MIG-7 generator is used to provide a IO constraint file, which is used to connect the required signals for the interface to the corresponding FPGA pins. The resulting schematic section regarding the interface connection of the memory chip is shown in figure 5.6

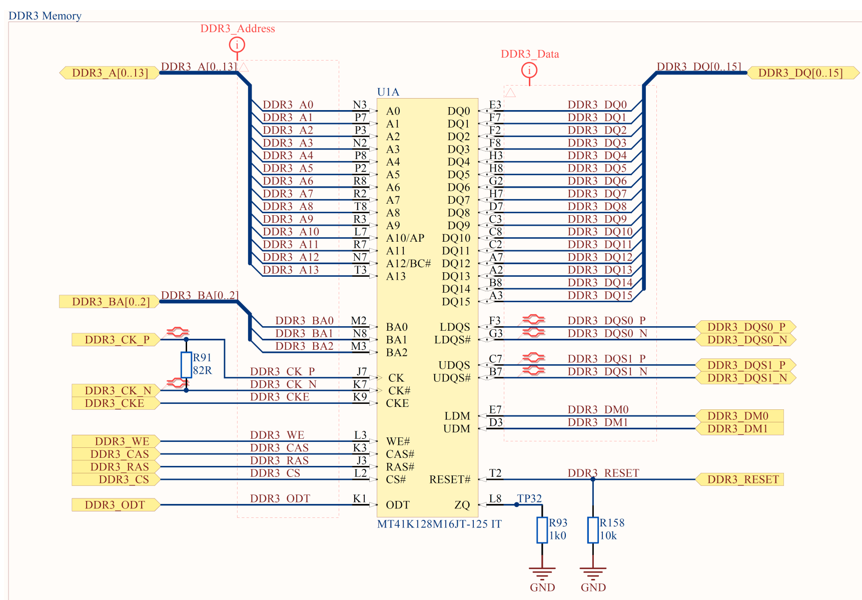


Figure 5.6: Schematic section of the DDR3 memory device

5.2.4 Camera Link Base

The Camera Link receiver chosen is the TI DS90CR288, which supports TTL clock rates of up to 85 MHz [11]. The data input consists of one LVDS pair clock input and four pairs of LVDS data inputs, which are terminated according to [8] with 100 Ω resistors. The LVDS nets are assigned into differential pairs and combined into the net-list LVDS_Base to allow for layout rules to be applied to all included signals.

To ensure local decoupling, ceramic capacitors are provided for each power pin. Furthermore a 4.7 µF tantalum bulk capacitor is added, as is recommended by the data sheet [11].

The resulting schematic section regarding the Camera Link base receiver is shown in figure 5.7.

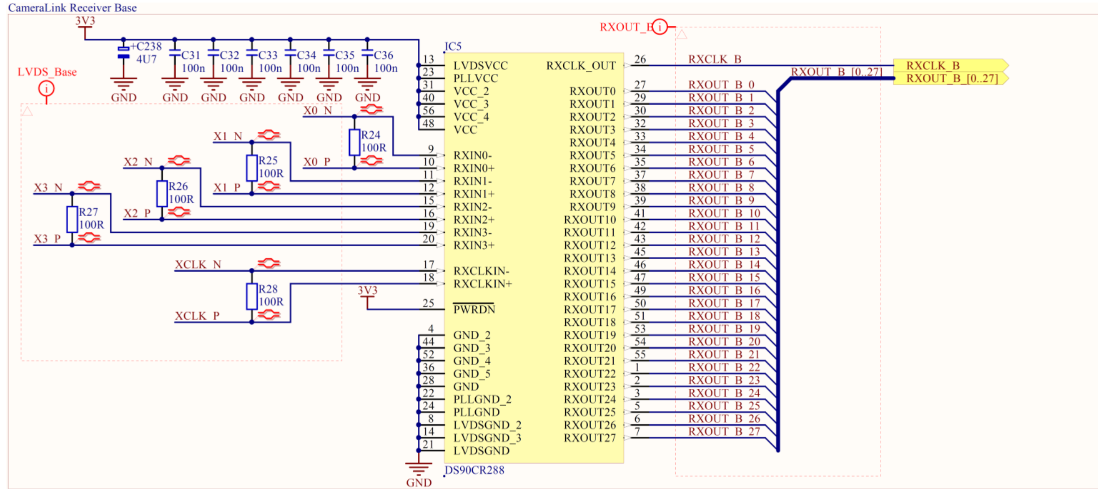


Figure 5.7: Schematic section of the Camera Link base receiver circuit

The implementation of the general control interface is done by using the TI DS90LV047, which is a four channel LVDS driver. It supports 3.3 V power supply and achieves data rates of up to 400 Mbit s^{-1} [41].

The asynchronous serial communication is handled by the DS90LV019 chip from TI, that consists of one LVDS line driver and one receiver. It supports data rates of 100 Mbit s^{-1} and complies with the Camera Link standard regarding the serial communication, which requires minimum data rates of 76.8 Mbit s^{-1} for the serial interface. [42]

5.3 PCB Planning

The aim of this section is the design of a suitable layer stackup for the PCB. This requires different factors to be taken into account, such as the required signal impedances, power supply layers and necessary via types.

Firstly, all high speed interfaces are evaluated regarding their requirements towards delay matching and trace impedances. Table 5.2 lists these interfaces and their physical layer specifications.

Table 5.2: Physical layer specification of high speed interfaces [8, 43, 44, 45]

Signal Type	Trace Length	Pair Matching	Group Matching	Trace Impedance	Differential Impedance
SATA	≤ 150 mm	2 ps	75 ps	$55\ \Omega \pm 15\%$	$90\ \Omega \pm 15\%$
LVDS	≤ 150 mm	2 ps	60 ps	$55\ \Omega \pm 15\%$	$100\ \Omega \pm 15\%$
USB	≤ 150 mm	25 ps	-	$50\ \Omega \pm 15\%$	$90\ \Omega \pm 15\%$
DDR3 Address	25-75 mm	-	25 ps	$50\ \Omega \pm 10\%$	
DDR3 Data	25-75 mm	-	15 ps	$50\ \Omega \pm 10\%$	

The pair and group matching parameters are determined by the skew margin proposed for the PCB. The trace impedances are determined to ensure minimised reflection losses induced by impedance mismatching, as specified in the corresponding data sheet.
The overall trace length recommendations are derived from the best practice guidelines [8, 46, 47].

Another aspect influencing the assessment of the layer stackup is the number of required signal layers.
Xilinx provides an estimative equation to determine the recommended minimal number of signal layers $N_{\mathsf{SignalLayers}}$ for the BGA fanout, equation 5.1. The number of routing channels $N_{\mathsf{RoutingChannels}}$ therein defines the total number of clearances between pads on the circumference of the selected BGA package. The routes per channel $N_{\mathsf{RoutesperChannel}}$ determine how many traces can be fitted between two neighbouring pads [46].
For the chosen 484-pad BGA package and the available number of signal pins $N_{\mathsf{SignalPins}}$ being 220, at least three signal layers should be provided.

$$N_{\mathsf{SignalLayers}} = \frac{N_{\mathsf{SignalPins}}}{N_{\mathsf{RoutingChannels}} \cdot N_{\mathsf{RoutesperChannel}}} = \frac{220}{84 \cdot 1} \leq 3 \tag{5.1}$$

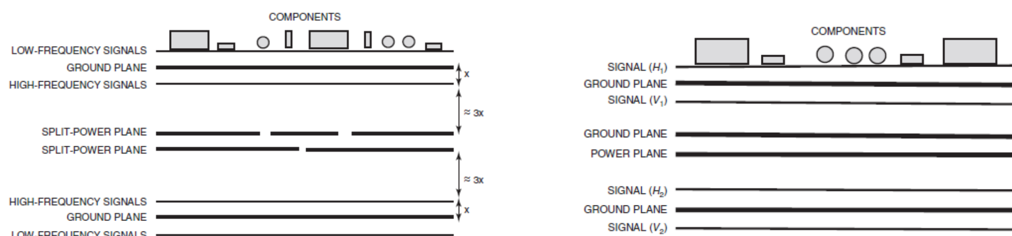
According to the estimation given in equation 5.1, the minimum number of signal layers is three.

Before specific layer stackups can be compared and evaluated, criteria for the rating of characteristics have to be defined. A conclusive system to rate and compare different stackups is presented by Ott in [48]:

1. Signal layers have an adjacent to plane.
2. Signal layers are close to an adjacent plane.
3. Power and ground planes are closely coupled together.
4. High-speed signals are routed on buried layers located between planes.
5. Multiple-ground planes are used, as they lower the impedance of the board and reduce common-mode radiation.
6. Critical signals routed on more than one layer are confined to two layers adjacent to the same plane.

With the amount of different power levels to supply the FPGA, a split plane is dedicated to the purpose of power supply adjacent to a solid ground plane.
To ensure the availability of buried signal layers purposed for high speed signals, signal layers between ground planes or between ground and power planes are required. To achieve a symmetrical stackup, with low speed routing layers on top and bottom, a minimum of four four signal layers is required. As a compromise between total number of layers and sufficient ground planes, an eight-layer stackup is proposed.

Ott in [48] provides the rating of two eight-layer stackups, figure 5.8. The high speed signal layers shown in figure 5.8a are not close to planes on either side. Also these signal layers are not located between planes, as they are situated beside a split power plane on one side.
The inner signal layers in figure 5.8b however are located between two solid planes, thereby complying with five out of six criteria.



(a) An acceptable eight-layer board stackup with four signal layers and two split power planes. This configuration satisfies four of the six objectives.

(b) An excellent eight-layer PCB stackup with good signal integrity and EMC performance. This configuration satisfies five of the six objectives.

Figure 5.8: Comparison of two different eight-layer stackups [48]

Taking these considerations into account, the stackup for the VADER project is chosen according to figure 5.9.
The inner core is bordered by a solid ground plane and the split power plane, while the outer cores contain the strip line layer and additional ground layers. The sandwiched cores are spaced by three layers of 1080 prepreg material. The outermost layers, intended for low frequency signals are also spaced by prepreg material, completing the eight layer stackup.

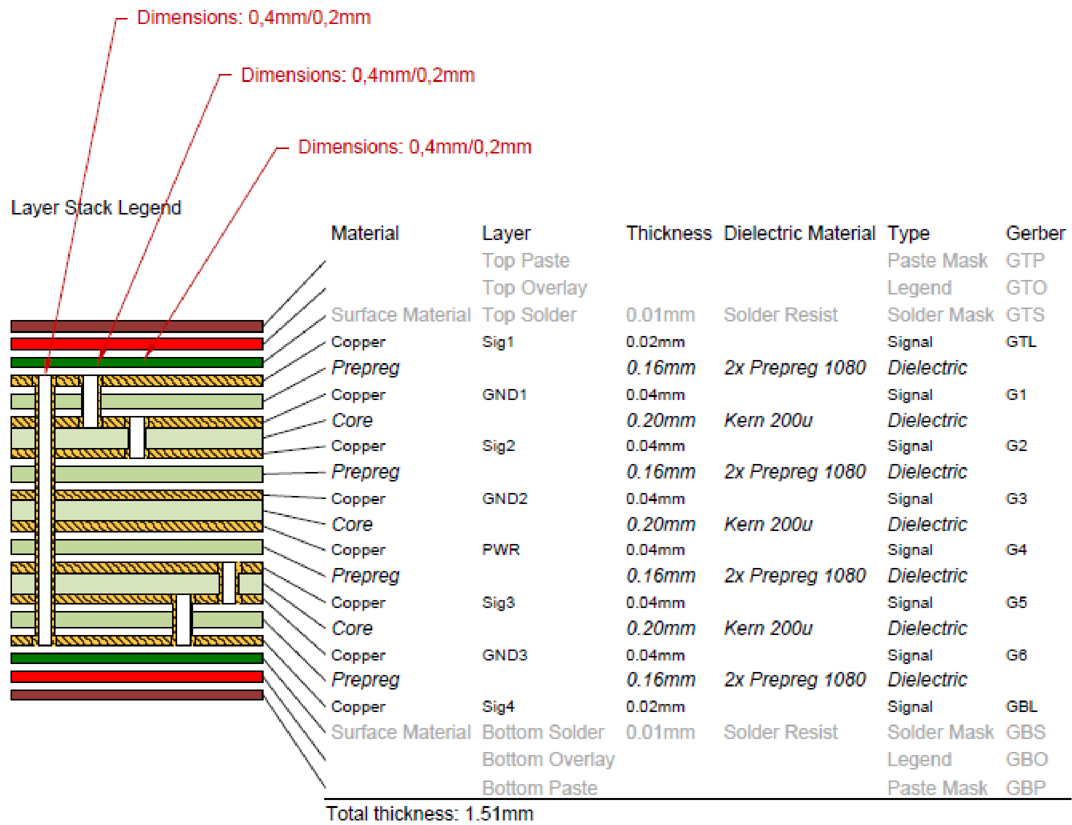


Figure 5.9: Layer stackup exported from the Altium Designer project

The given stackup fulfils four out of the criterion for all layers. However the first internal signal layer Sig2 intended for high speed signals complies with the demand for two adjacent planes, meeting criterion six for same plane ground reference, fulfilling five out of six criteria.
To minimise EMI effects the high speed signals are preferentially routed on Sig2. To minimise parasitic effects of via stubs, staggered micro vias are inserted into the design, inherent to the physical dimensions of the dielectrics and the given 1:1 size ratio, figure 5.9 [49]. With the dimensions of the layers determined and the producibility verified by the PCB manufacturer [50], the necessary trace geometries can be calculated.
The estimations provided in chapter 2 are used to determine the required widths. The results are then compared to the output of Saturn PCB. The resulting trace geometries for the four signal layers and the high speed interface signals are listed in table 5.3.

Table 5.3: Trace dimensions for critical interfaces per layer

	SATA		LVDS		USB		DDR3
	55 Ω	90 Ω	55 Ω	100 Ω	50 Ω	90 Ω	50 Ω
	Width	Spacing	Width	Spacing	Width	Spacing	Width
Sig1	220 µm	143 µm	220 µm	240 µm	270 µm	270 µm	270 µm
Sig2	100 µm	120 µm	100 µm	230 µm	150 µm	220 µm	150 µm
Sig3	100 µm	120 µm	100 µm	230 µm	150 µm	220 µm	150 µm
Sig4	220 µm	143 µm	220 µm	240 µm	270 µm	270 µm	270 µm

5.4 Layout

The description of the layout phase is done for the key system elements, the decoupling and fanout of the FPGA, the DDR3 memory interface as well as the Camera Link base circuitry.
As the development of the layout is an iterative process being subject to common sense optimisation and simulation based verification, the layout sections discussed in the following are the results of the implementation after aforementioned optimisations. The documentation of the simulation-based optimisations are described in chapter 6.

5.4.1 FPGA

The layout implementation of the FPGA section is done in the following iterative sequence [39]:

1. PWR-plane polygons
2. Capacitor placement
3. Power Distribution Network (PDN) analysis
4. GTP transceiver circuits
5. DDR3 interface
6. Camera Link interface
7. Fanout low speed signals

Firstly, the PWR plane polygons are created, making sure the vias connecting the FPGA pads are embedded within the according plane. The resulting polygon arrangement under the FPGA is shown in figure 5.10. The vias connecting the supply and GND pads of the BGA package are laid out to be 1 mm spaced to adjacent power pins to ensure that the 100 nF 0402 capacitors can be placed directly beneath the package with minimal parasitic inductance. All further capacitors are placed in the perimeter of the FPGA, also to minimise the resulting parasitic inductance.

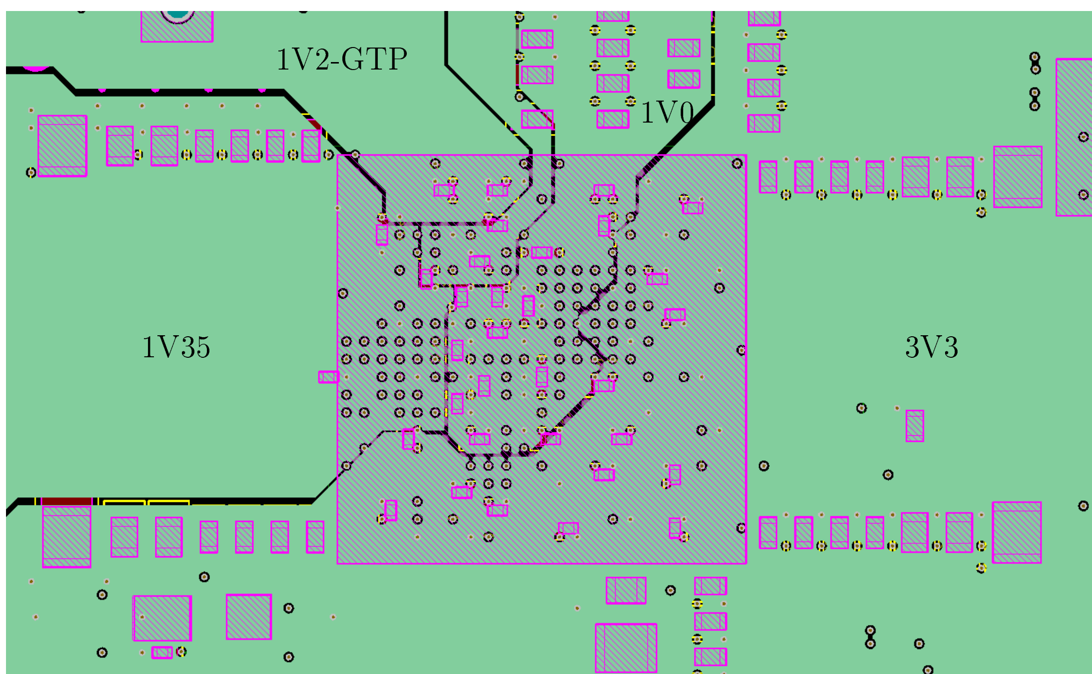


Figure 5.10: Implemented PWR-plane, showing net polygons as well as placed decoupling capacitors

To verify the effectiveness of the decoupling, a PDN analysis is conducted [51]. To estimate the amount of AC-voltage ripple on a given power rail, a LTspice simulation is used (Appendix A.1.10). It consists of the capacitor modelling according to section 2.2 with a calculated via inductance according to section 2 of 0.6 nH for the implemented stackup. Furthermore, the capacitance of the given power supply polygons is taken into account according to equation 5.2, as a function of the polygons area A_{polygon}, the core thickness d_{core} and the dielectric constant ϵ_{R} of the core material.

$$C_{\mathsf{polygon}} = \epsilon_0 \epsilon_{\mathsf{R}} \frac{A_{\mathsf{polygon}}}{d_{\mathsf{core}}} \tag{5.2}$$

To estimate the target impedance, Bogatin in [52] gives equation 5.3, which divides the maximum ripple voltage for the supply rail V_{ACripple} by the estimated maximum ripple current set at 50 % of the maximum current consumption.

$$Z_{\mathsf{target}}(f) \leq \frac{V_{\mathsf{ACripple}}}{0.5 \cdot I_{\mathsf{max}}} \tag{5.3}$$

The power consumption for the 1V0 rail is estimated with the power supply estimation tool provided by Xilinx (Appendix A.1.6) with a fabric usage of 70 %. The resulting maximum supply current for the core-voltage I_{max} is thereby given as 2 A. Taking the allowable AC ripple of 50 mV for the core voltage into account, the target impedance of the 1V0 net is calculated to be 50mΩ (Appendix A.1.3).

To find the maximum frequency at which the board level decoupling is effective, as opposed to the die-decoupling, Bogatin [52] gives an estimation based on the ratio of lead inductance of the FPGA supply to target impedance. With a calculated lead inductance for the FPGA of 0.6 nH and target impedance of 50 mΩ the maximum board level decoupling frequency of 100 MHz is adopted [52].
The resulting impedance plot for the 1V0 net as a function of frequency as a result of the simulation is shown in figure 5.11. The target impedance of 50 mΩ up to a frequency of 100 MHz is depicted as dashed line.
The impedance curve for frequencies below 1 kHz is not further analysed, as the switch mode power supplies can compensate voltage ripples within these frequencies.
As the target impedance is met for the specified frequency range up to 100 MHz, the amount of decoupling for the 1V0 power rail is considered to be sufficient.

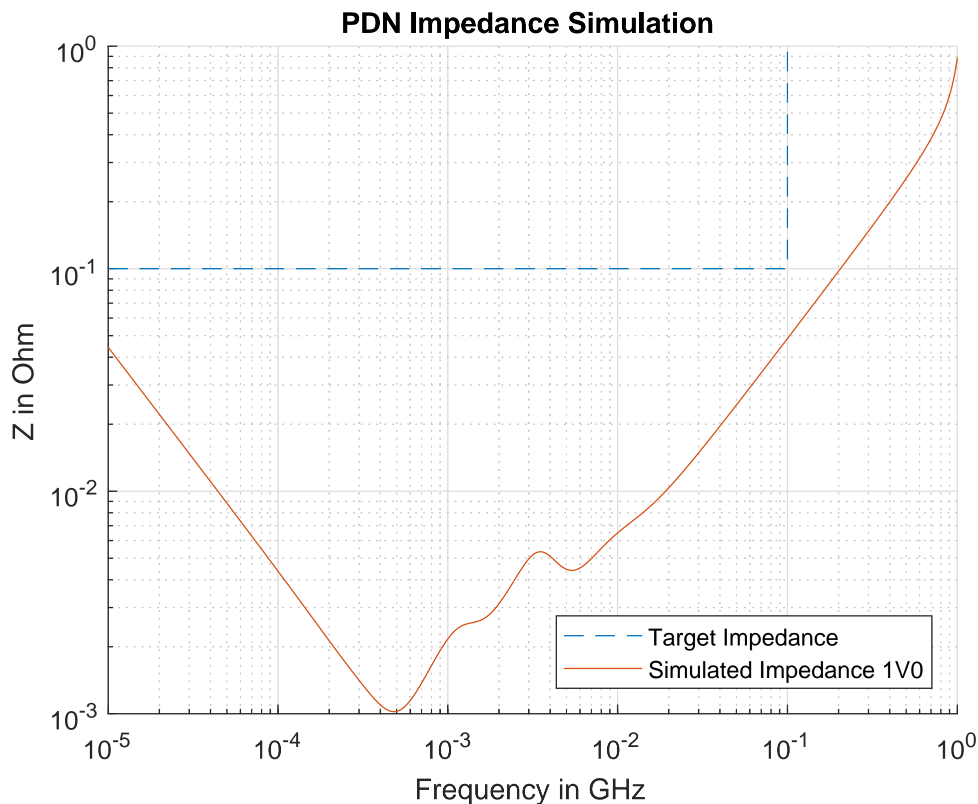


Figure 5.11: Simulated impedance of the 1V0 PDN

5.4.2 DDR3

The next step in the layout process is the routing of the DDR3 traces.
As recommended in [53] the data group and the address and control group are routed on different stripline layers, with the data lanes traced on the Sig2 layer, as they posses the highest bandwidth signals and the shielding provided by two adjacent GND planes is beneficial. They are grouped into data bytes with the differential data strobe pairs in the middle. The crosstalk effects as a function of spacing between adjacent signal traces is analysed in section 6.

Address lines, control signals and the differential clock signal are routed on layer Sig3. They are matched to ±1 mm according to the skew margin, table 5.2. As Sig3 is located between a GND plane and the split power-plane, the signals are only traced under the 1.35 V supply polygon, figure 5.12, to ensure noise suppression.

The placement of the decoupling capacitors for the memory chip is done according to the recommendations given by the manufacturer, [43]. Figure 5.12 shows the implemented layout of the DDR3 signal traces on layers Sig2 and Sig3 with stashed polygons for better visibility of the traces.

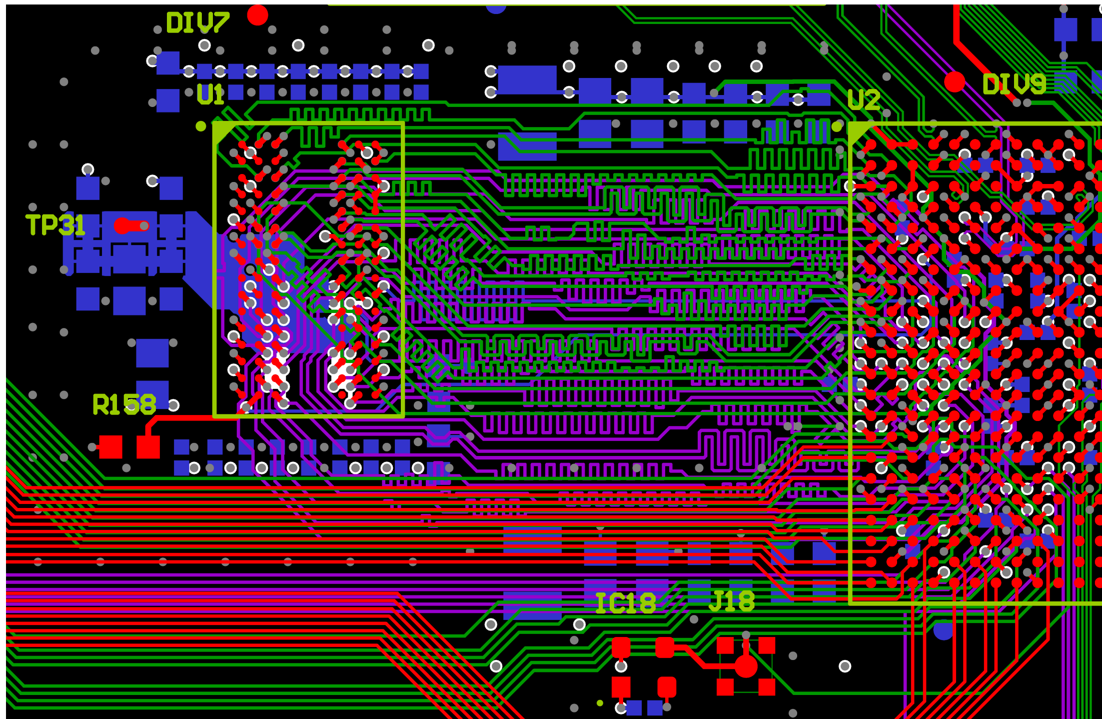


Figure 5.12: Implemented data traces (green) and address traces (purple) between DDR3 memory chip U1 and FPGA U2

5.4.3 Camera Link Base

The Camera Link Base circuitry consists mainly of the receiver chip, connector, the control and serial interface chips, with the critical traces being the LVDS pairs.

The termination resistors, required by the LVDS standard are placed as close as possible to the receivers to minimise the unterminated stub lengths. To meet the length matching requirements, table 5.2, the differential pair length matching rules are set to ± 2.54 mm (Appendix A.1.7), calculated with the propagation delay estimation for layer Sig1.

To minimise propagation differences within the channels caused by partial traces on inner layers, the staggered micro vias in the traces connecting Sig2 to the top layer Sig1 are placed as close as possible to the connector, figure 5.13.
As described in the schematic section, decoupling capacitors are placed at every power pin. To minimise the loop area, they are placed on the back side of the PCB. The 3.3 V are provided through the power plane. Figure 5.13 shows the resulting layout section of the Camera Link base circuitry, showing traces on layers and polygons Sig1 and Sig2 with stashed polygons.

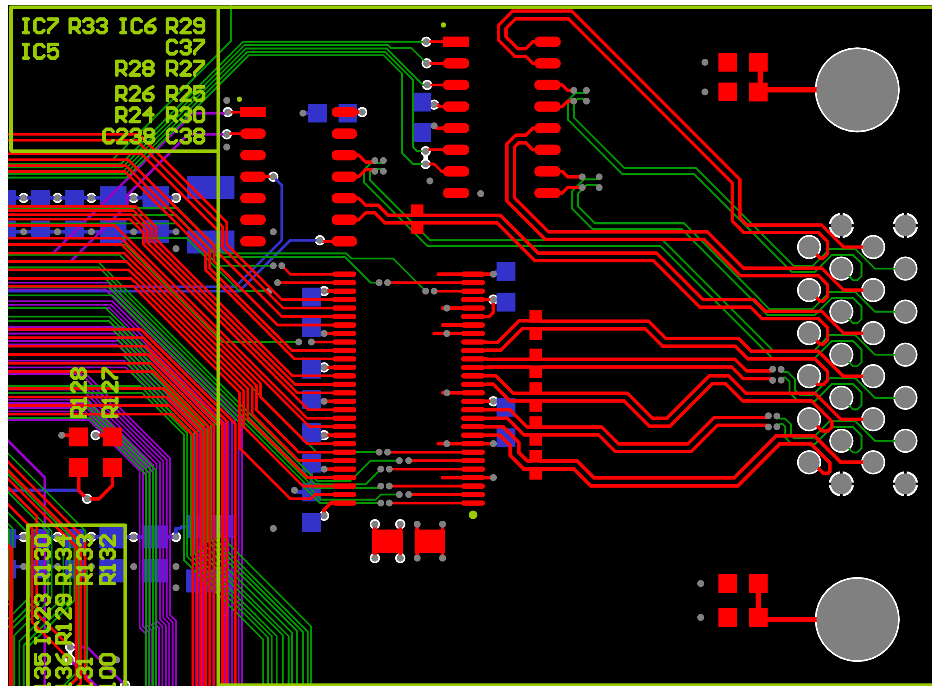


Figure 5.13: PCB section of the Camera Link base group

5.5 Resulting PCB

With the critical high speed interfaces in place, the low speed signal traces are routed. Firstly the remaining signals are fanned out from the FPGA and then connected to the system elements. The resulting PCB layout is shown in figure 5.14. To display all placed signal traces, all polygons are stashed. Also for traceability of the system elements, the components of a given system element are enclosed by silkscreen rectangles.

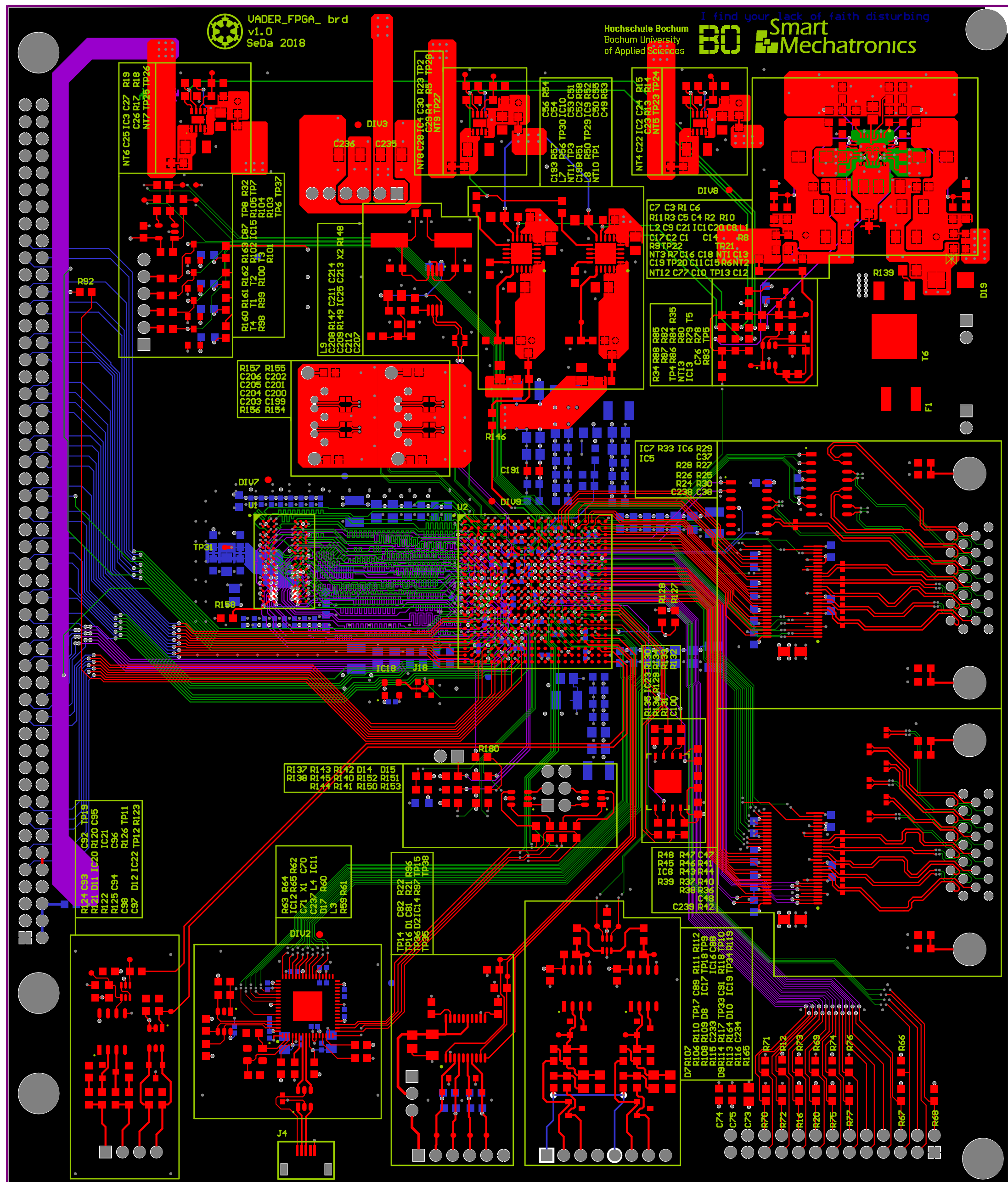


Figure 5.14: Resulting PCB highlighting traces on signal layers

6 Simulation

The aim of using a 3d field simulation program as post layout validation is to ensure that the signal integrity requirements are met with the designed PCB. Therefore S-parameters are calculated for a given set of traces, which can be used to generate eye diagrams for given signals [54].
The software used is the CST microwave studio version 2018. The simulation environment is set up using the guides available in [54].
The proposed work flow is to import the layout from the Altium designer via ODB++ manufacturing data, including layer stackups and passive component values. To optimise the duration of the simulation, the nets that are analysed are cut out of the full PCB, with spacing of 10 mm to the selected traces, maintaining a rectangular cut-out [55]. The simulation analysis is described for the DDR3 crosstalk estimation, the SATA 3 Gbit s^{-1} signal integrity analysis as well as the documentation of the optimisation of the Camera Link base LVDS channels.

6.1 DDR3

The simulation of the DDR3 interface is aimed to verify that the crosstalk between data lines is within the specification, by analysing the s-parameters linked to the crosstalk parameters. The simulation is conducted for the data lines DQ5 and DQ7, as they are located in the center of the data line bus and the documentation of the analysis is representative of all lines.
The schematic configuration of the crosstalk simulation is depicted in figure 6.1, showing the configuration of the ports. The ports 1 and 3 are located on the pads of the DDR3 memory chip, while the ports 2 and 4 are placed on the FPGA pads. The s-parameters of interest for the crosstalk behaviour are the S_{41} and S_{23}, as they define the far end crosstalk for two data lines.

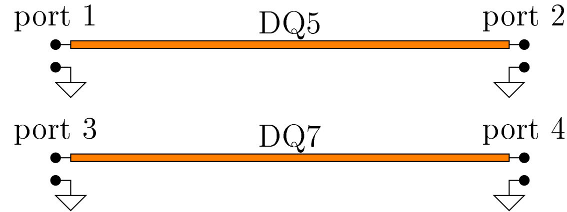


Figure 6.1: Port description of the crosstalk measurement

Figure 6.2 shows the highlighted data lines DQ5 and DQ7 in the CST environment. They consist of staggered micro vias connecting the BGA pads on the top layer Sig1 to the stripline traces routed on layer Sig2. The four specified wave-ports are referenced to the ground net, with an impedance of 50 Ω. Port 1 and port 3 emerge from the DDR3 chips pads, while port 2 and port 4 are connected to the BGA pads associated to the FPGA chip.

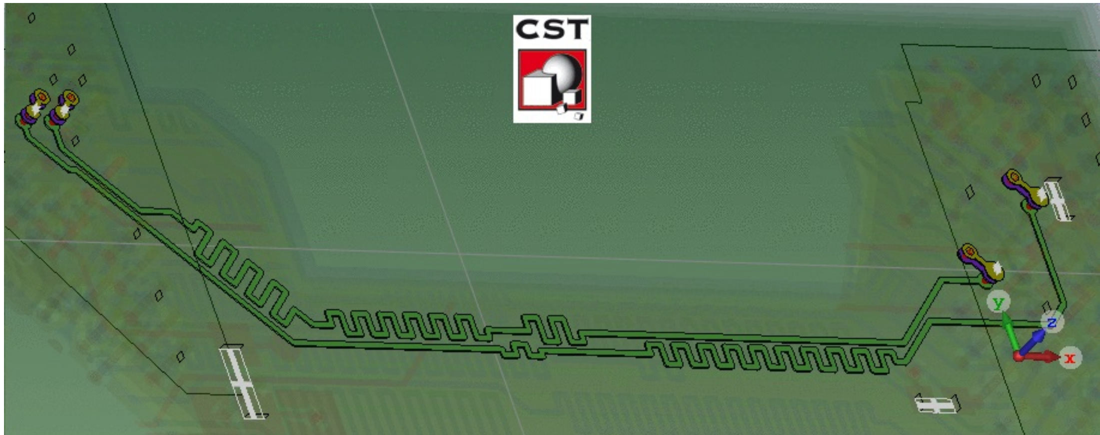


Figure 6.2: Image of tested DDR3 Data Lines DQ5 and DQ7 on Signal Layer 2

To estimate the maximum bandwidth at which to ensure the crosstalk margin is met, the maximum rise time of the data signals is necessary.
The data sheet lists the maximum occurring signal slew-rate as 12 V ns^{-1}, which leads to a maximum rise time of 112.5 ps, when considering the power supply voltage of 1.35 V. [38]
Using the bandwidth estimation given as $BW = 0.35/T_{\text{rise}}$ by Johnson in [13], the maximum occurring frequency of the DDR3 signals is 3.11GHz.

The maximum crosstalk voltage injected from one channel into a neighbouring channel is selected to be 5 %, leading to a maximum magnitude of the crosstalk relevant s-parameters S_{41} and S_{21} as −26 dB, equation 6.1.

$$S_{\mathsf{max}} = 20 \cdot \log(5\ \%) = -26.02\ \text{dB} \tag{6.1}$$

The results of the conducted crosstalk simulations are depicted in figure 6.3, showing the S_{41} and S_{21} parameters for three different spacings between data lines DQ5 and DQ7. The initial spacing is set to 100 µm, resulting in magnitudes of the crosstalk parameters exceeding the −26 dB limit.

For the second iteration, the spacing rules for the data lines and address lines are increased to 150 µm and all traces are re-routed to comply.

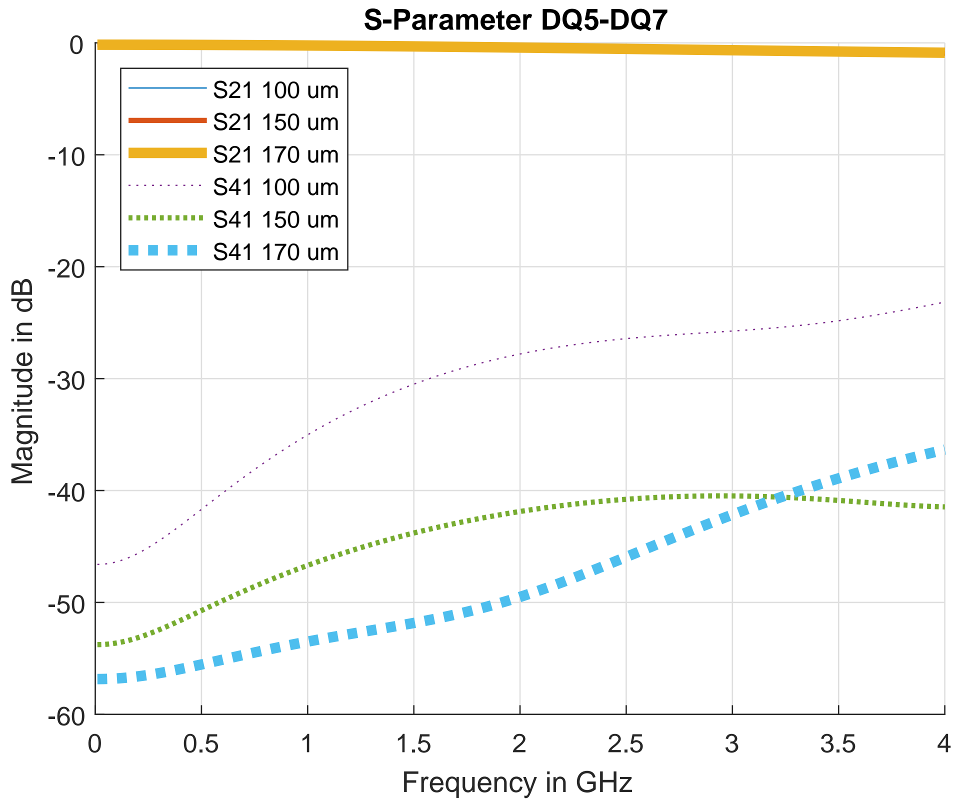


Figure 6.3: Simulated s-parameters of DQ5 to DQ7 data lines, with spacings of 100 µm, 150 µm and 170 µm

As figure 6.3 shows, the increased spacing leads to a significant reduction of the crosstalk parameter of almost −10 dB throughout the frequency range of interest.

Even though the required crosstalk dampening of 26 dB is now met throughout the specified frequency range, the layout arrangement allows an increase of the trace spacing to 170 µm. This modification is also conducted to analyse the behaviour of the crosstalk. The result is depicted in figure 6.3 as the thickest dotted line, which further improvements the behaviour of the crosstalk in the frequency range up to 3.11GHz.

As the crosstalk margin for the interface is met, the next simulated analysis is the evaluation of an eye diagram simulation for a data lines. The main parameter of interest in this simulation is the undershooting and overshooting behaviour of the signal.

The data sheet of the selected DDR3L memory chip specifies the maximum overshoot peak amplitude as 0.4 V with the maximum overshot area above V_{DD} as 0.25 V ns, figure 6.4. The maximum peak undershoot amplitude and maximum undershoot area are defined with the same numerical values.

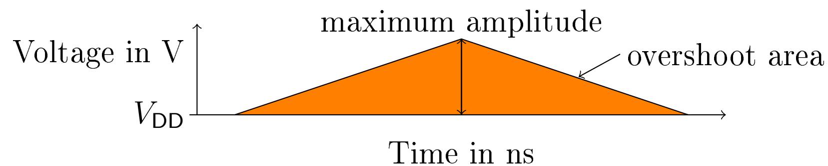


Figure 6.4: Definition of overshoot amplitude and area for DDR3L clock and data pins [38]

The simulated eye diagramm for the DQ7 data line is shown in figure 6.5. The maximum overshoot and undershoot amplitudes are 0.31 V, meeting the required maximum of 0.4 V. The measured overshoot and undershoot areas are 0.0325 V ns, also within the defined specification.

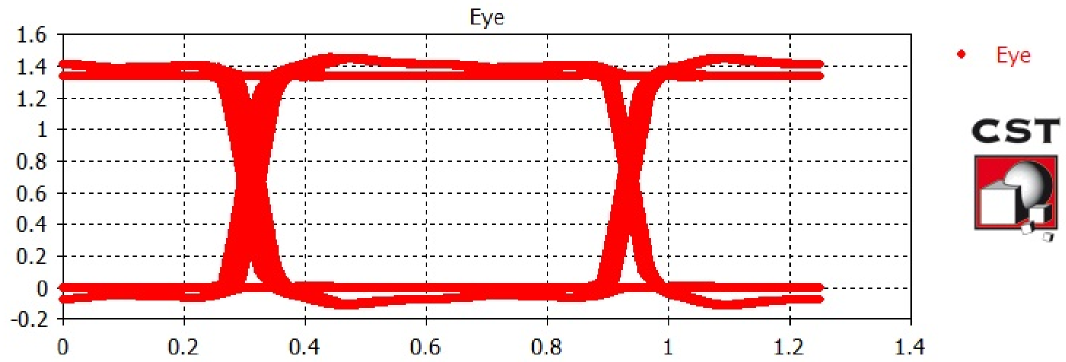


Figure 6.5: Simulated Eye Diagram DQ7, period: 625 ps, rise and fall time: 60 ps, amplitude: 1.35 V

6.2 Sata RX

The SATA-interfaces possess the highest requirements with regard to signal bandwidth. The maximum bandwidth arises from the signals maximum occurring rise and fall time of 67 ps for the SATA 3 $\mathrm{Gbit\,s^{-1}}$ Gen2 standard [47].
The resulting maximum bandwidth for the SATA signals can thereby be estimated as 5.22 GHz.

The analysed differential trace is highlighted in figure 6.6. The connector is visible to the left, with ac-coupling capacitors mounted on the top side. The stripline traces are routed on layer Sig2 due to the ground planes on both sides.

Figure 6.6: Analysed SATA traces, SATA_RX2

To ensure correct function of the interface, the transmission parameters S_{21} and S_{12} for the differential data lines are to be kept below -3 dB of attenuation up to the maximum signal bandwidth. As an example, the documentation of the simulation process is done for the RX trace of the SATA 2 interface, as the initial simulation results show the highest transmission attenuation exceeding the -3 dB above frequencies of 4.5 GHz, figure 6.6.

As the set transmission requirements are not met, the proposed optimisation is the rearrangement of the staggered micro via arrangement of the FPGAs fanout, figure 6.7. The initial via arrangement has the second stage microvias from the ground plane to the Sig2 layer placed directly under the corresponding BGA pad.
The optimised fanout rotates the traces on the ground pane, leading to the positioning of the second microvias stage to be under the opposed pad of the data pair.

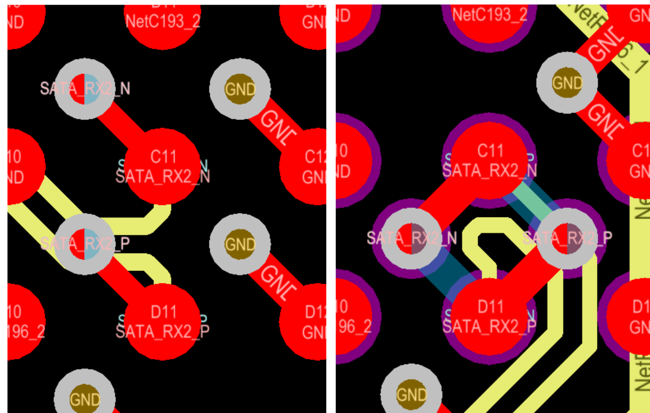


Figure 6.7: Optimisation of the FPGA fanout for the differential SATA traces

The simulation results of both fanout arrangements can be compared in figure 6.8. The optimisation, plotted in thicker lines, leads to an improvement in the attenuation coefficient S_{21}, meeting the requirements up to the frequency of maximum bandwidth of 5.22 GHz. Figure 6.8 also shows the reflection coefficient limits given by the SATA standard in [47], which is fulfilled with the optimised fanout of the SATA traces.

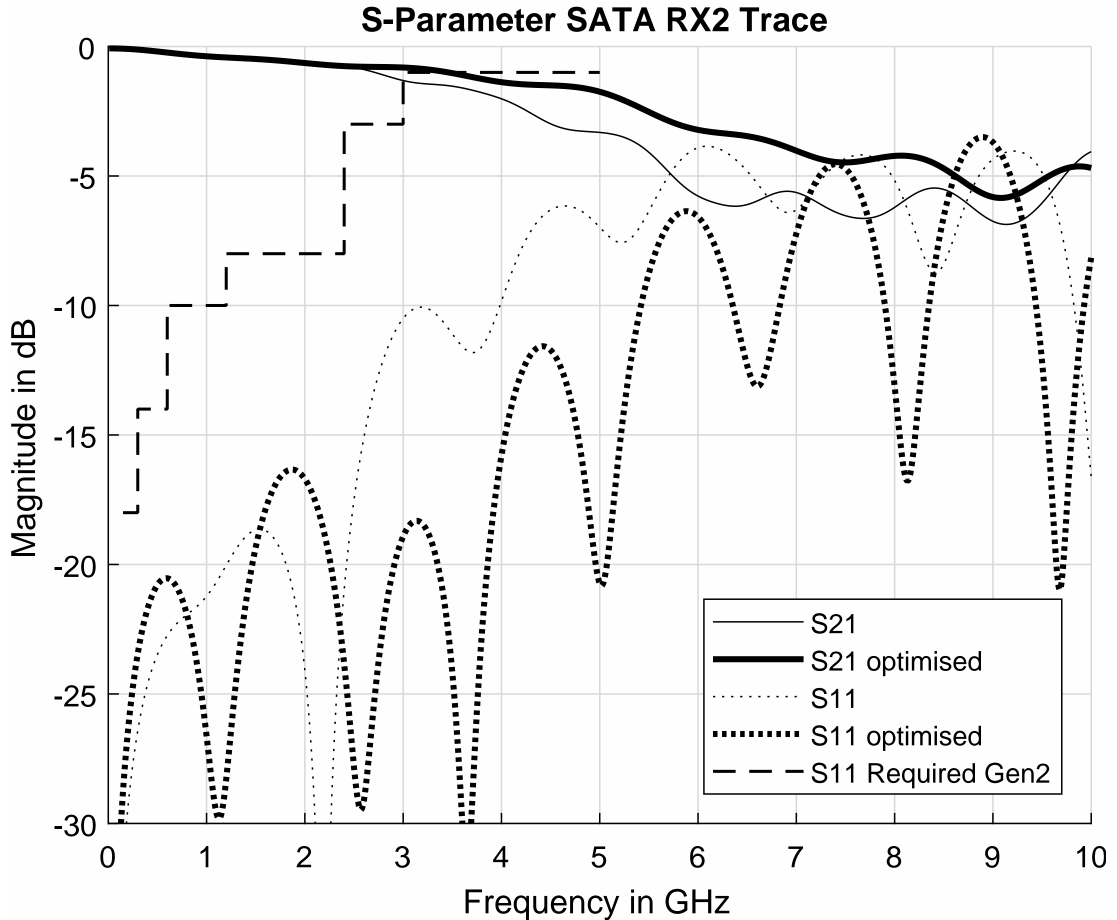


Figure 6.8: Simulated s-parameters of the Sata Rx Channel 2 Port comparing pre and post optimisation results

To simulate the signal integrity of the SATA traces, an eye diagram is simulated according to the signal specifications given by the SATA standard in [47]. For the SATA 3 $\mathrm{Gbit\,s^{-1}}$, the signal period is setup with 330 ps, while the rise time of 67 ps is applied. The amplitude of the signal at the transmitter is 400 mV. To account for transmitter jitter the duty cycle jitter is set to 0.05 % unit interval [47].

The resulting eye diagram is depicted in figure 6.9, which shows overshoot and undershoot of 25 % after the level transients, which are within the specification. The valid data region spans ± 120 mV, which is also achieved. The resulting eye width also complies with the requirements that the SATA 3 $\mathrm{Gbit\,s^{-1}}$ standard specifies, as the maximum jitter does not exceed 50 ps. [47]

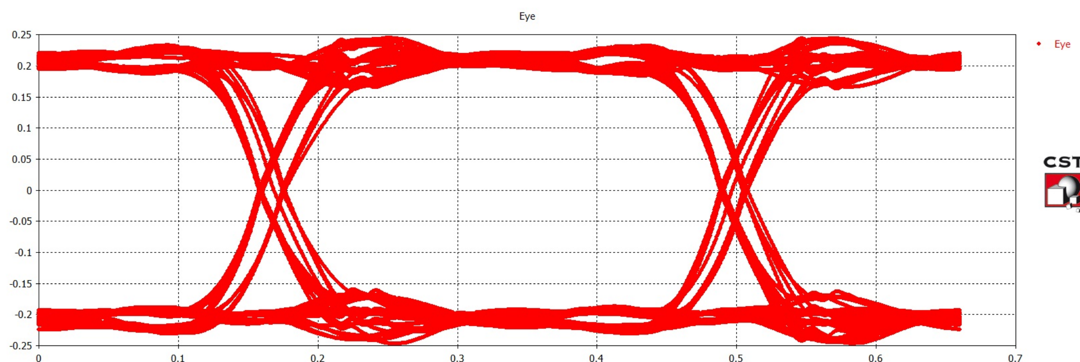
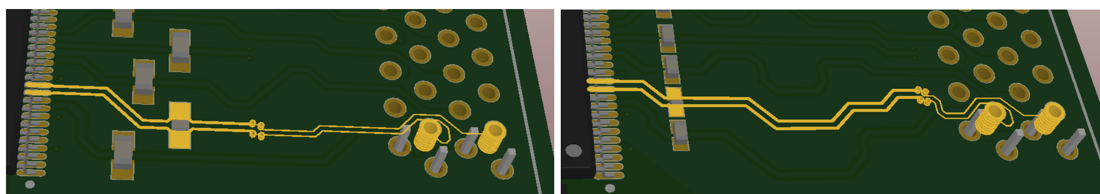


Figure 6.9: Simulated eye diagram using SATA 3 Gbit s^{-1} standard signal setup

6.3 Camera Link base

To verify the signal integrity of the Camera Link interface during the simulation phase, all Camera Link related LVDS channels are analysed. The documentation is done representatively for the X1 channel of the Camera Link base receiver.
The maximum bandwidth of the Camera Link signals arises from the specified maximum rise time of the LVDS data signal, which is 750 ps resulting in a bandwidth of 467 MHz. The differential traces of the X1 LVDS link implemented during the first iteration of the layout are shown in figure 6.10a. The traces comprise the 100 Ω termination resistor in a 0603 package.
The s-parameter simulation for the initial link is shown in thin lines in figure 6.11. The transmission losses average to 3.5 dB within the specified frequency range. The reflection losses show a minimal attenuation of −9.3 dB. The targeted limits of 3 dB of admission losses and 10 dB of reflection attenuation are not met.



(a) Initial layout of Camera Link channel X1 (b) Improved layout of Camera Link channel X1

Figure 6.10: Comparison of Camera Link channel X1 pre and post optimisation

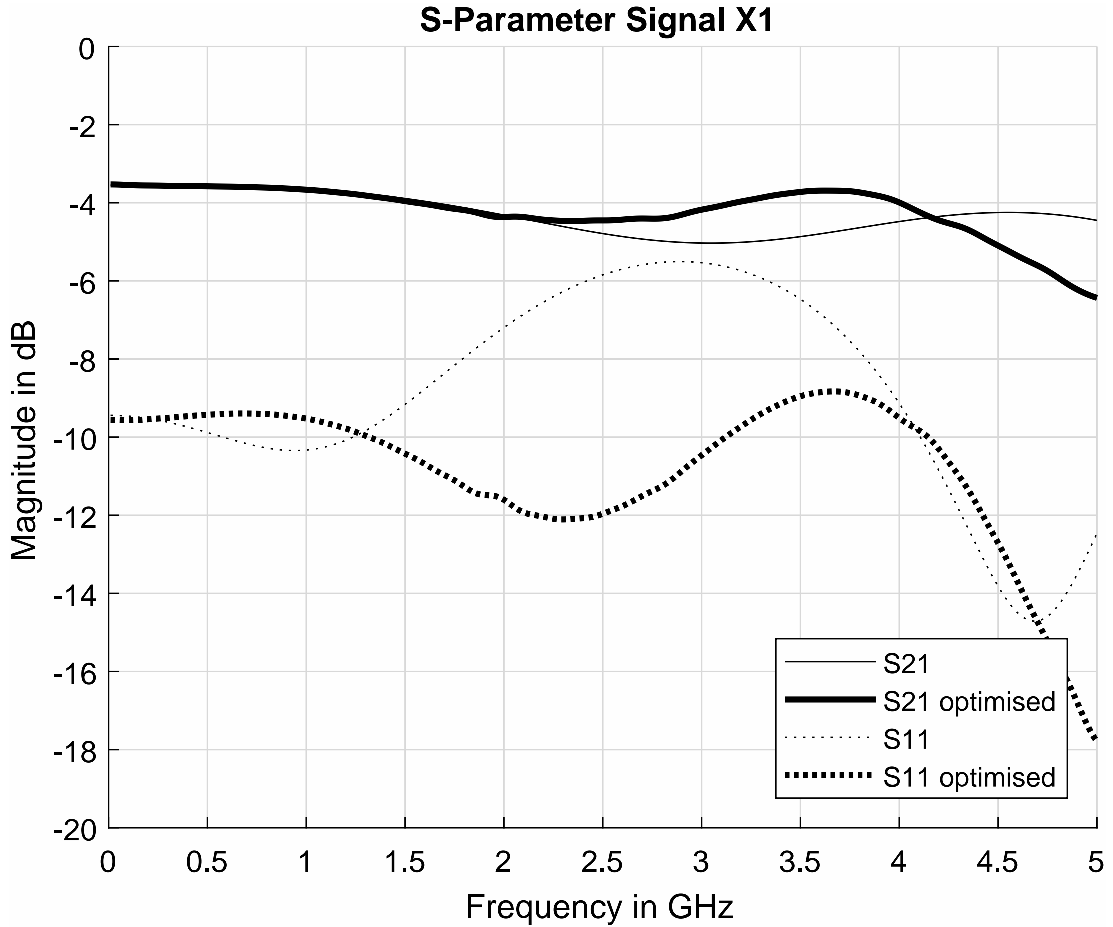


Figure 6.11: S-parameter simulation of LVDS channel X1 with 100 Ω termination

The proposed optimisations are depicted in figure 6.11. The 0603 package termination is changed into a 0402 package, allowing for decreased unterminated stub length. Furthermore the via transition from Sig2 to Sig1 is moved closer to the Camera Link connector.

The resulting simulation results are shown in figure 6.11, as thick lines.
As figure 6.11 indicates, significant improvements in both reflection coefficient and admission coefficient occur at frequencies above 1.2 GHz, however the behaviour within the specified bandwidth up to 467 MHz is unchanged.
Even though the determined limits are not achieved after the optimisation, the signal integrity simulation in form of an eye diagram simulation is carried out.

The resulting eye diagram, simulated for a bit period of 1.68 ns with a rise time of 0.75 ns and an amplitude of 290 mV is shown in figure 6.12, according to the Camera Link receiver data sheet [11]. The jitter percentage of 0.089 % used to setup the simulation is derived from the data sheet, taking a 1 m cable and the given transmitter jitter into account.

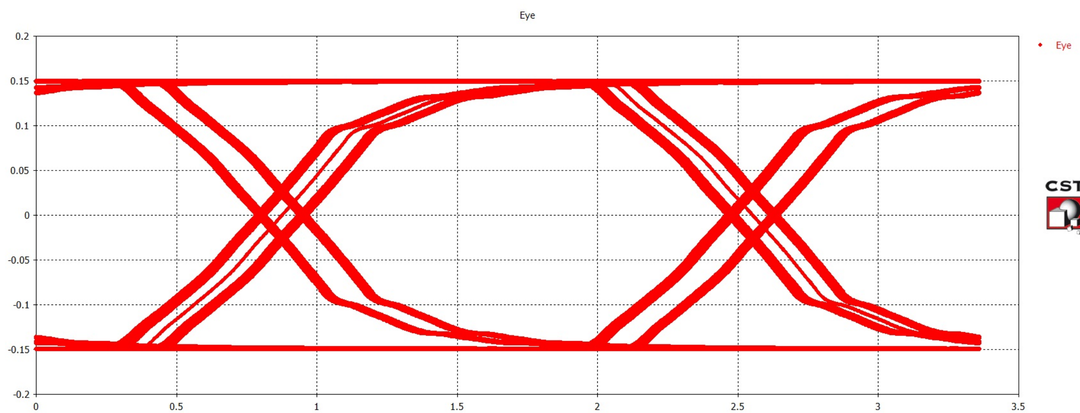


Figure 6.12: Simulated eye diagram LVDS channel X1

The required eye width of 0.7 ns for the differential input threshold voltage of 100 mV is achieved by the simulation carried out for the optimised layout of channel X1. As the eye diagram shows, the signal integrity of the link fulfils the signal integrity requirements, the Camera Link interface passes the simulation phase.

7 Verification

This chapter describes the the verification process of the completed PCB. The tests are executed according to the test plan (Appendix A.1.5) generated during the implementation phase.
The testing is divided into functional groups, beginning with the verification of the power supply system. The next step is the testing of the FPGA circuitry. Furthermore, the verification of the s-parameter simulation of the DDR3 interface is conducted. Finally the correct function of the low speed interfaces is verified.

7.1 Power-Supply

To ensure that none of the components mounted on the PCB are damaged by incorrect voltage levels, all net ties located at the outputs of the voltage converters are disconnected.
The open circuit voltage outputs of all power rails are then measured, according to the test plan and compared to the requirements regarding each rail, table 7.1.

Table 7.1: Voltage measurements of power rails for open circuit and 20 % FPGA usage

Power rail	Requirement	Open circuit	**20% device usage**
1V0 VCCINT	0.95 V – 1.05 V	1.007 V	1.006 V
1V8 VCCAUX	1.71 V – 1.89 V	1.809 V	1.801 V
3V3 VCCO	2.97 V – 3.45 V	3.345 V	3.342 V
5V0	4.75 V – 5.25 V	5.024 V	5.005 V
1V35	1.283 V – 1.45 V	1.345 V	1.340 V
1V0 GTP	0.97 V – 1.03 V	1.009 V	1.005 V
1V2 GTP	1.17 V – 1.23 V	1.208 V	1.201 V

With all power rail meeting the requirements of the specified voltage levels, the start-up behaviour of the rails is analysed. The setup time for each rail is compared to the specified start-up window according to the requirements, Appendix A.1.3. The documentation of the sequence verification is done using a four channel oscilloscope, with the trigger set to the input power supply to ensure that all measurements can be displayed in a single diagram. The resulting plot is shown in figure 7.1. The main voltage rails are ramped coincidently, reaching their specified voltage levels within the timing constraint. Also the linear voltage regulators for the GTP-transceiver are enabled by the power-good output of the 5V0 rail and achieve the specified timing requirements.

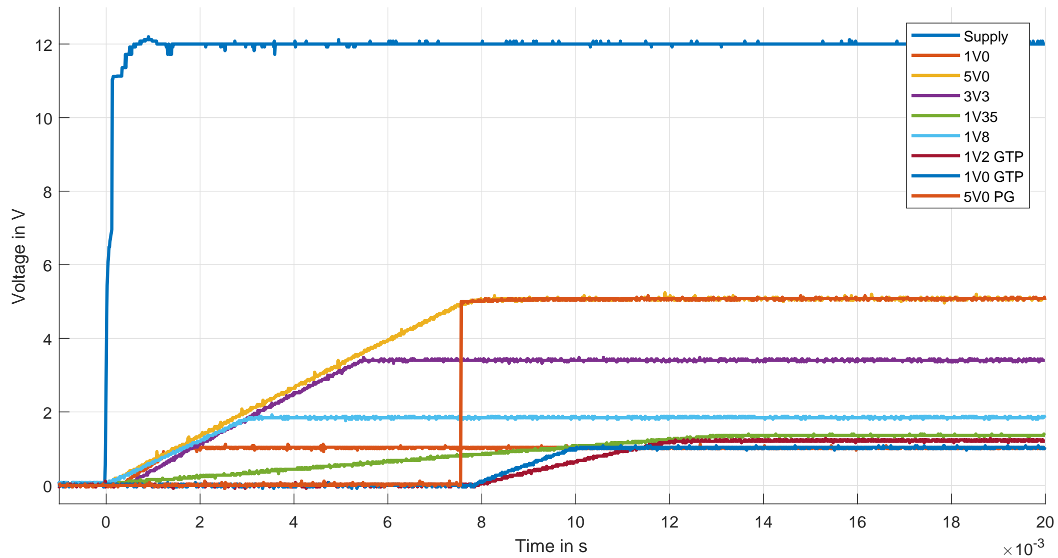


Figure 7.1: Verified power supply start-up sequence of the FPGA board

7.2 FPGA

The first step in verifying the correct behaviour of the FPGA is the JTAG boundary scan, using the Vivado Suite. As the Artix-7 device shows up in the connected devices list with the correct ID, the next step is the programming of a bit-stream file (Appendix A.1.8).

The initial test program divides the connected oscillator clock signal of 100 MHz down to a 100 kHz signal, which is used to toggle the connected debugging LEDs. This verifies the JTAG interface of the FPGA as well as the connected oscillator. The created constraint file used to verity the interfaces connected to the FPGA is attached as verification project, Appendix A.1.8.

7.3 Camera Link

To verify the correct function of the Camera Link interface, the test pattern mode of the Dalsa Spyder3 is used, as specified within the test plan (Appendix A.1.5). To set the camera into test mode, two of the LED expansion header pins are configured as links to the Camera Link serial interface, allowing for the external connection of a USB-to-Serial converter. This enables the communication with the camera via a terminal program on a computer, to manually review the cameras status [56].

The test pattern created by the camera is shown in figure 7.2, containing a number of 1024 12 bit pixel values, in which the first half increments from 0 to 511 and the second half decreases from 4095 to 3584. A verification program is written for the FPGA which compares the received frames to the expected pattern, counting the number of detected differences (Appendix A.1.9).

The verification is conducted over a duration of 30 min, leading to a total number of $1.8 \cdot 10^8$ received and compared camera test frames. Throughout the test, no errors are detected while comparing the camera data to the expected results.

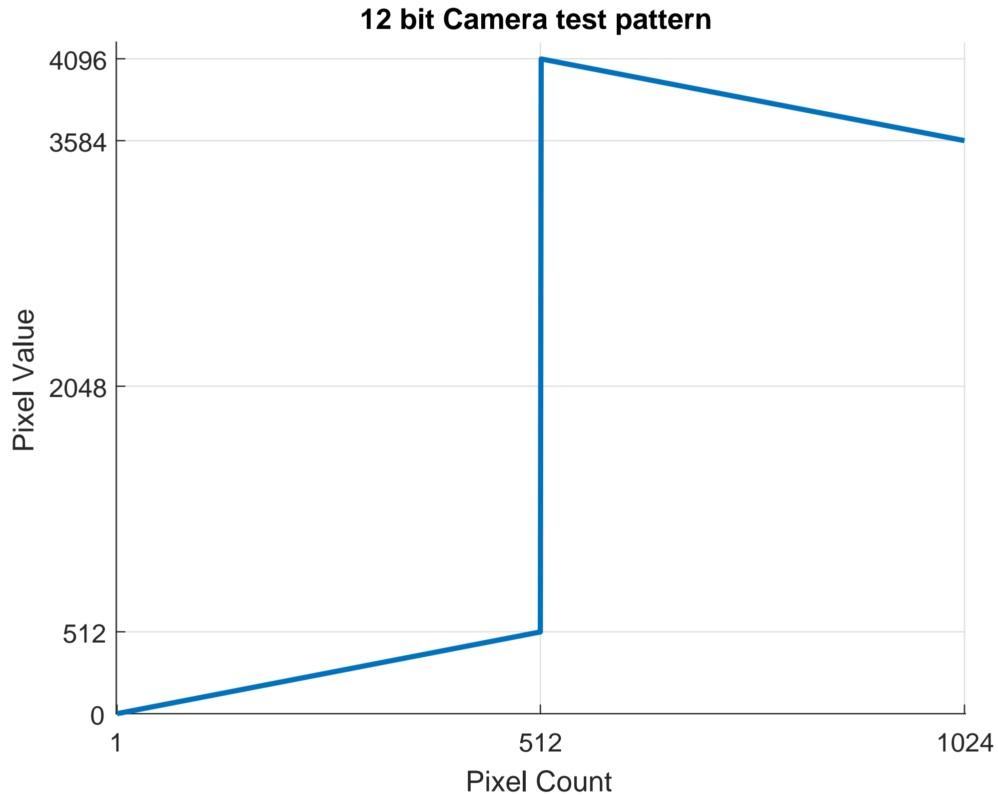
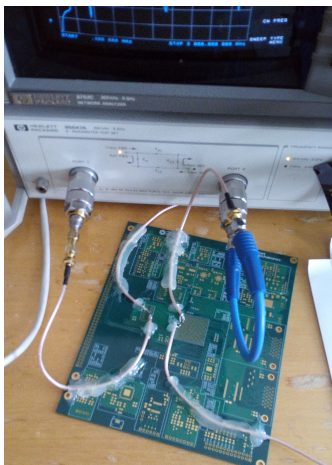


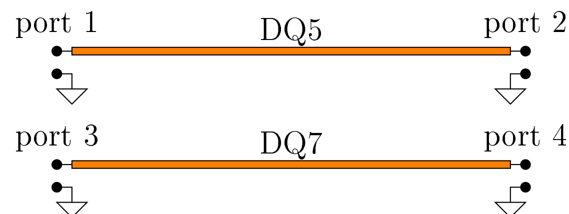
Figure 7.2: Generated test pattern image created by the Dalsa Spyder3 camera

7.4 DDR3

The verification of the physical layer of the DDR3 interface is done by measuring the s-parameters of the signal traces similar to the simulated results. The experimental setup is shown in figure 7.3a, with the unpopulated PCB connected to the vector network analyser. The Ball Grid Array (BGA) pads of the FPGA and the DDR3 chip are soldered to SMA based cables, with the cable shield soldered to a ground pad in close proximity. Figure 7.3b shows the schematic setup of the measurement, with ports 1 and 3 located at the DDR3 memory.



(a) Physical setup of the measurement



(b) Schematic setup of the s-parameter measurement

Figure 7.3: DDR3 s-parameter measurement setup and schematic

The measured s-parameters are depicted in figure 7.4, with the parameters of interest for the far end crosstalk being the S_{14} and S_{23} s-parameters. The measurement of the multi port s-parameters is conducted according to [57]. The frequencies analysed within the measurement range from 300 kHz to 3 GHz, defined by the utilised measuring device. The lowest crosstalk suppression rates −28 dB for a frequency of 1.05 MHz.
The simulation results with the lowest crosstalk parameter of −40 dB are not precisely reproduced. Calculating the resulting crosstalk percentage according to equation 7.1 yields 3.98 %. The required 5 % required as maximum crosstalk between the channels DQ5 and DQ7 is thereby met. Taking the setup of the measurement into account in regards to the soldered SMA cables, the result seems reasonable.

$$FEXT = 10^{\frac{-27\ \mathrm{dB}}{20}} = 3.98\ \% \tag{7.1}$$

The forward transmission coefficients show a maximum admission of −10 dB for the S32 parameter at 2.5 GHz. The simulated maximum admission however rates −3 dB. A possible reason could be the SMA cables used. Therefore the cables used for the measurement are soldered together and the transmission coefficients are measured directly and plotted in figure 7.4 as a dotted line showing a maximum dampening of 5 dB.

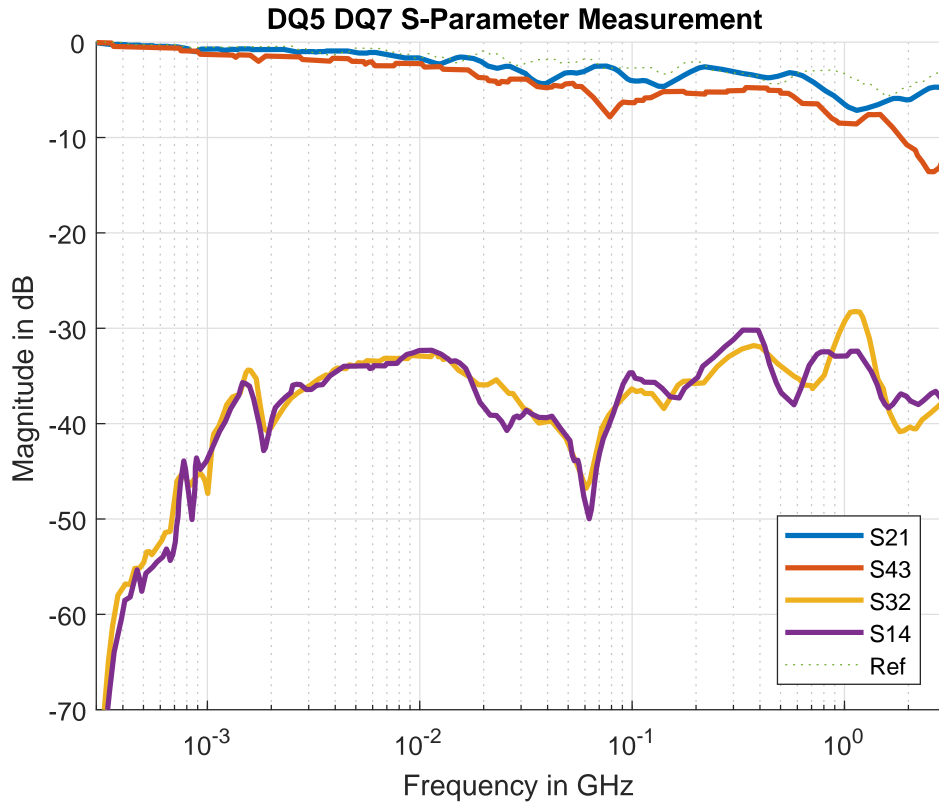


Figure 7.4: Far end crosstalk measurement between data lines DQ5 and DQ7

As the DDR3 interface cannot be tested via software at the point of the completion of the thesis, the correct function of the interface cannot be verified, however the conducted measurements verify the qualitative plausibility of the simulation.

7.5 Low-speed interfaces

The unit tests and integration tests of the low-speed interfaces are conducted according to the test plan document generated during the system design phase.

The populated PCB used to verify the interfaces is shown in figure 7.5.

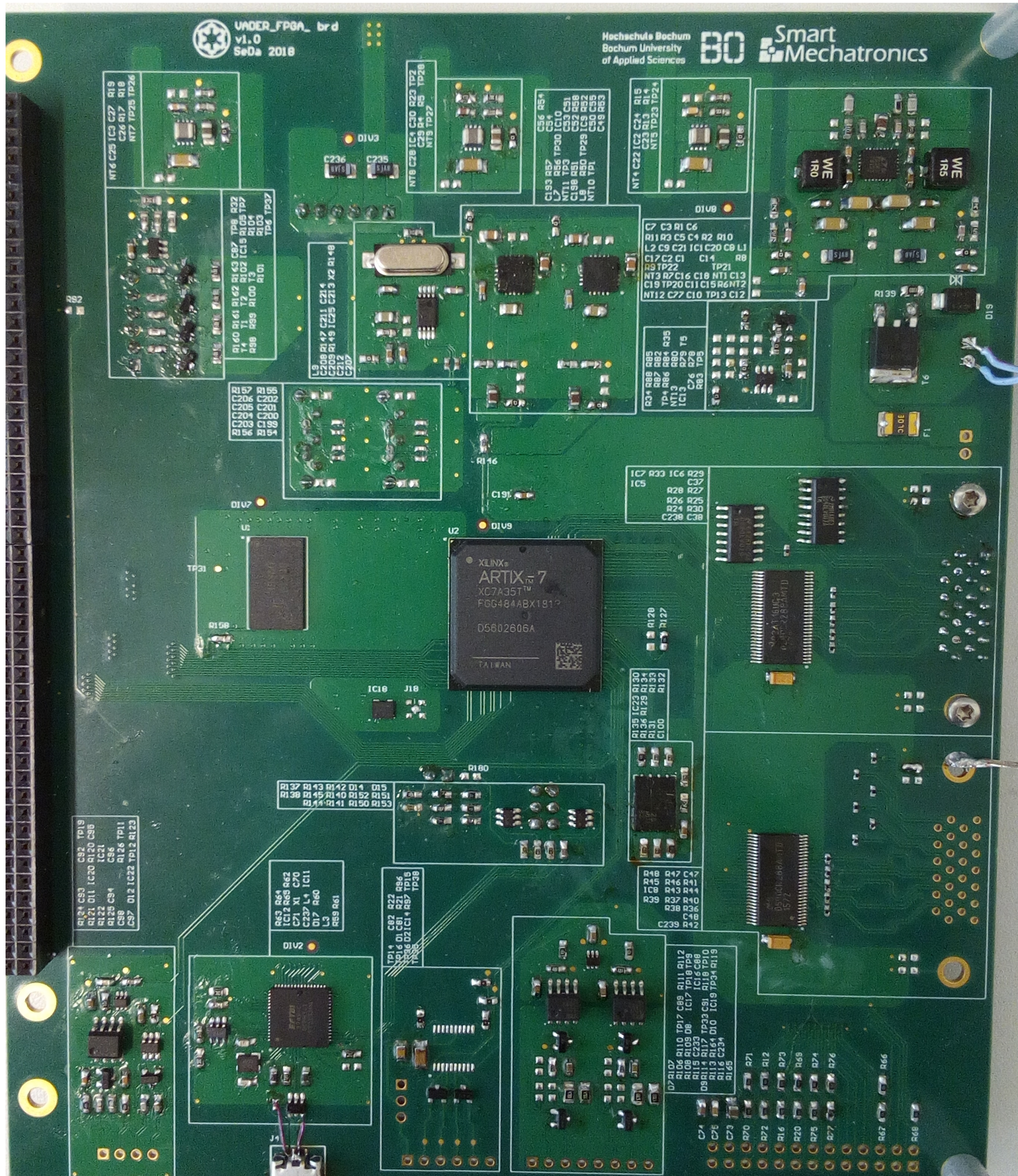


Figure 7.5: Resulting PCB used for the verification

The chronological order of system element verifications executed is listed in the following, with all results recorded in the test plan, Appendix A.1.5:

- USB Interface: Verify the configuration of the FT2232H chip and test the bidirectional data transfer between the FPGA and a computer with an example program, Appendix A.1.8.

- SSI interface: Verify the correct conversion of the differential clock input to a TTL output signal and measure the differential output of the data channel at the maximum specified frequency of 2 MHz.
- Photo sensors: External 24 V signals are applied to the input of the photo sensor circuitry and the output voltage of the circuitry is measured and compared to the specified output.
- Temperature sensor: The verification is conducted by reading a temperature value via SPI from the mounted temperature sensor chip and comparing the read value to the measurement of a suitable thermometer.

8 Conclusions

The aim of this project was the development of a hardware platform to evaluate advanced spatial filter algorithms, which was achieved during the project. The project included the requirements engineering of the complete system, the elaboration of hardware specific requirements, the assessment of a suited system architecture as well as the implementation and validation of a custom hardware prototype.

Verifying theoretical calculations using simulations in an early stage of the implementation phase, relying on a milestone-based project schedule as well as the post layout simulation loop led to the verified custom electronics hardware board usable for its main purpose.

Even though the majority of the test specified in verification were successful, the correct function of the high speed interfaces was not verified, as the complete verification was optionally agreed upon (Appendix A.1.1). The correct function can only be estimated through the simulation results and s-parameter measurements. The final verification must be conducted in a future software based project by frame error rate testing [19].

With the necessary functionality for the hardware prototype verified, the enhancement of spatial filter algorithms can be conducted. For a future hardware project combining DSP, FPGA and peripherals into a single PCB, the selected board stackup can be used. Furthermore the PDN analysis for the DSP can be conducted analogue to the described analysis. Furthermore, if the attached improvement list, Appendix A.2, is taken into consideration, the design risk of the combined hardware development can be minimised.

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A Appendix

A.1 Data-CD

1 Documents\Projektauftrag_VADER_BRD.pdf

2 Documents\Lastenheft_SFV_V1.0_freigegeben.pdf

3 Documents\Anforderungen_Spannungsebenen.pdf

4 Documents\Meilensteinplan_VADER.pdf

5 Documents\Testplan.xls

6 Calculations\Powersupply\

7 Calculations\Implementation \

8 Verification\Hello_World\

9 Verification\Cameralink \

10 Simulation\PDN\

11 Datenblätter\

12 AltiumProject \

13 Masterthesis\Masterthesis_Dalton

14 Schematic \VADER_FPGA_Schematic.pdf

15 Documents \AnordnungFPGA_BRD.pdf

A.2 Errata

1. 100 Ω series resistor in McASP traces must be increased to 330 Ω for the first prototype
2. Camera Link connector BOM order number must be changed to 517-10226-6212PL
3. BOM order number of DS90LV047 has to be changed to correct footprint part
4. Footprint of NUM60 digital-transistor must be updated
5. FTDI JTAG connection must have 0 Ω resistors in series
6. With SMD PCB assembly only, Micro-USB connector has no mechanical attachment and must be soldered by hand
7. SPI Flash should be changed to an Artix-7 Vivado compatible manufacturer device
8. GND test points should be added next to system elements circuits

A.3 Schematic

CameraLink_Base
CameraLink_Base.SchDoc
DIN_S
DE_S
ROUT_S
RE_S
DINC[1..4]
ENC
RXCLK_B
RXOUT_B_[0..27]

CameraLink_Medium
CameraLink_Medium.SchDoc
RXCLK_M
RXOUT_M_[0..27]

CON_DSP
CON_DSP.SchDoc
MCASP0AHCLKX
MCASP0ACLKR
MCASP0AMUTE
MCASP0FSR
MCASP0AXR[0..15]
MCASP0FSX
MCASP0ACLKX
MCASP0AHCLKR
MCASP1ACLKX
MCASP1FSR
MCASP1AXR[0..9]
MCASP1ACLKR
MCASP1FSX
MCASP1AMUTE_R
MCASP1AHCLKR
SPI2_CLK
SPI2_SCS0
SPI2_MISO
SPI2_MOSI
RESETSTAT

Mechanical
Mechanical.SchDoc

USB_INTERFACE
USB_INTERFACE.SchDoc
FTDI_RXF
FTDI_TXE
FTDI_WR
FTDI_RD
FTDI_SIWUA
FTDI_D[0..7]
FTDI_OE
JTAG_TDI
JTAG_TDO
JTAG_TCK
JTAG_TMS

FPGA_ALL
FPGA_ALL.SchDoc
INP_B
INP_A
SSI_CLK
SSI_DTA
INC_B
MON_INC
INC_A
MASTER_RESET
ANY_GIP1
ANY_TX
ANY_OM1
ANY_RESET
ANY_MI0
ANY_GOP1
ANY_MI1
ANY_IRQ
ANY_GOP0
ANY_RW
ANY_OE
ANY_GIP0
ANY_OM0
ANY_OM2
ANY_LED1A
ANY_RX
ANY_LED2B
ANY_MD0
ANY_CE
ANY_LED2A
ANY_LED1B
LD[1..4]
TEMP_SC
TEMP_SI
TEMP_CS
TEMP_SO

SENSOR_INPUT
SENSOR_INPUT.SchDoc

SSI
SSI.SchDoc

INCREMENTAL
INCREMENTAL.SchDoc

Voltage_Monitor
Voltage_Monitor.SchDoc
PG_1V0_GTP
PG_1V2_GTP
PG_5V0
PG_DDR3_1V35
PG_1V8
PG_3V3
PG_1V0
MASTER_RESET

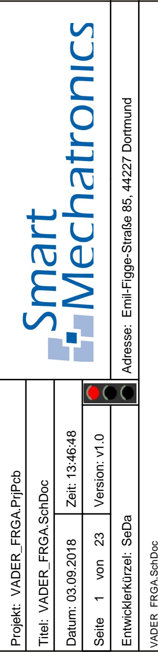
LDO_GTP
LDO_GTP.SchDoc
LDO_EN
PG_1V0_GTP
PG_1V2_GTP

BUCK_TPS82140
BUCK_TPS82140.SchDoc
PG_5V0
PG_DDR3_1V35
PG_1V8

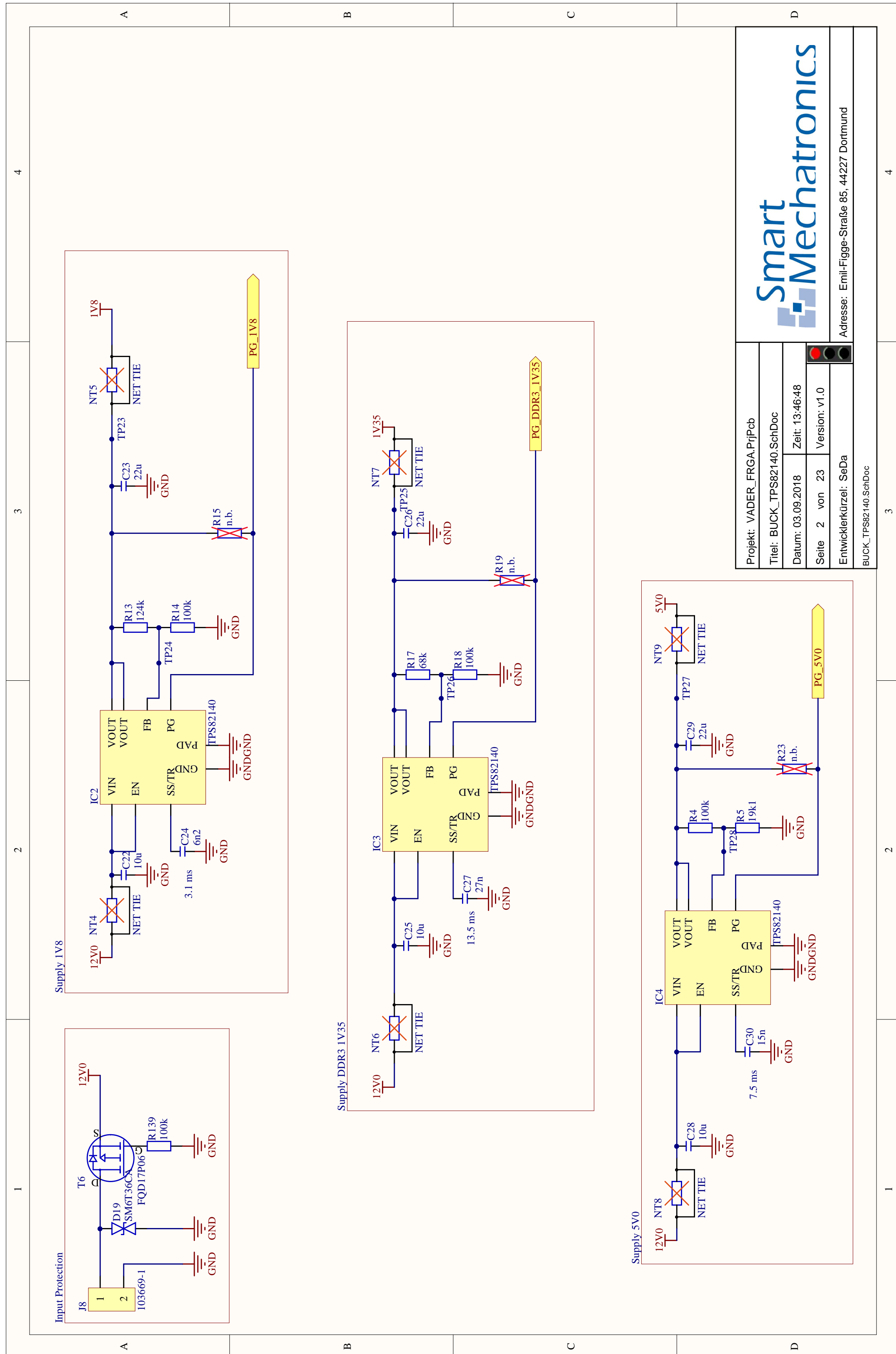
BUCK_LTC3636
BUCK_LTC3636.SchDoc
PG_3V3
PG_1V0

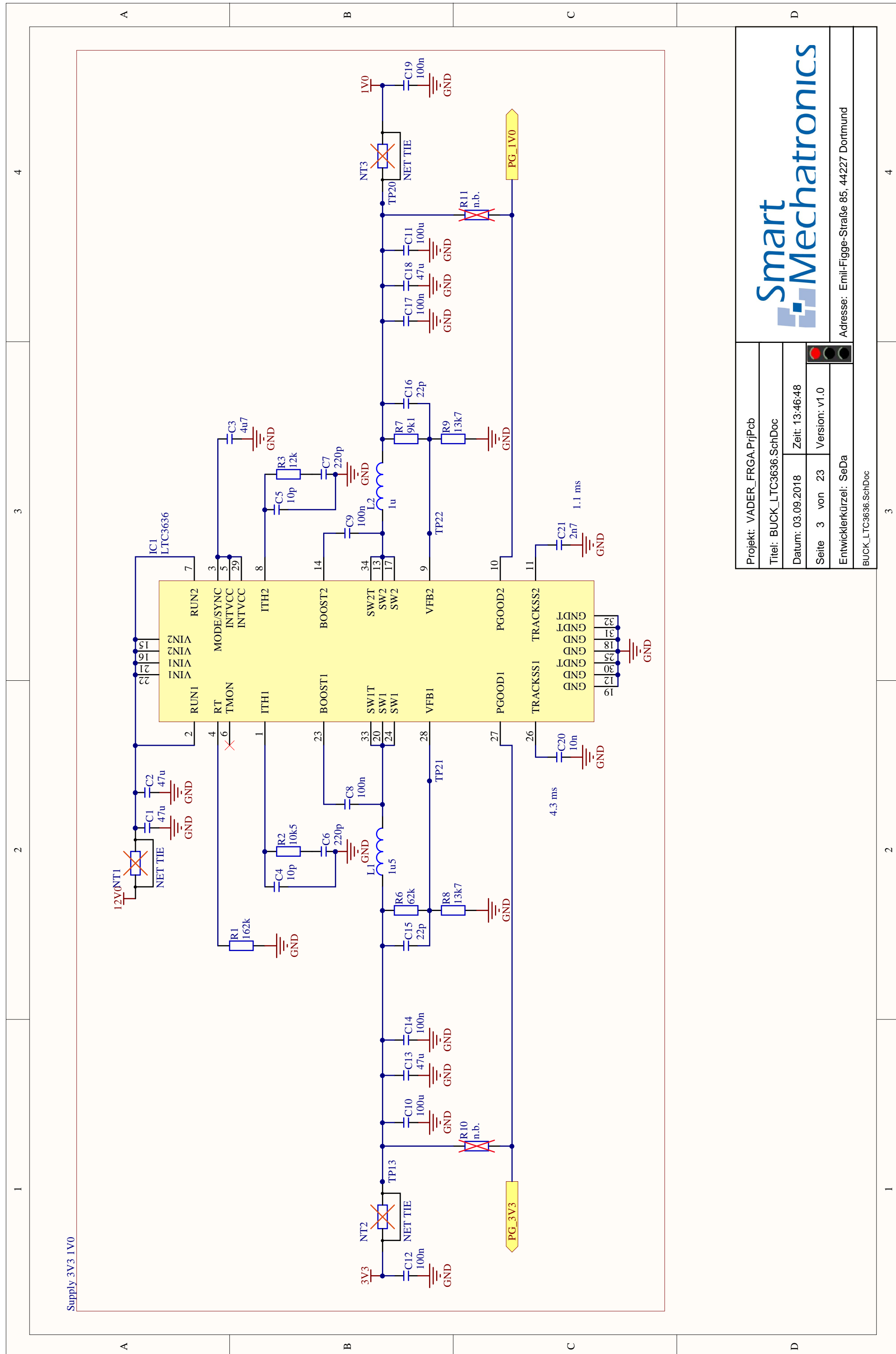
AnyBus
AnyBus.SchDoc

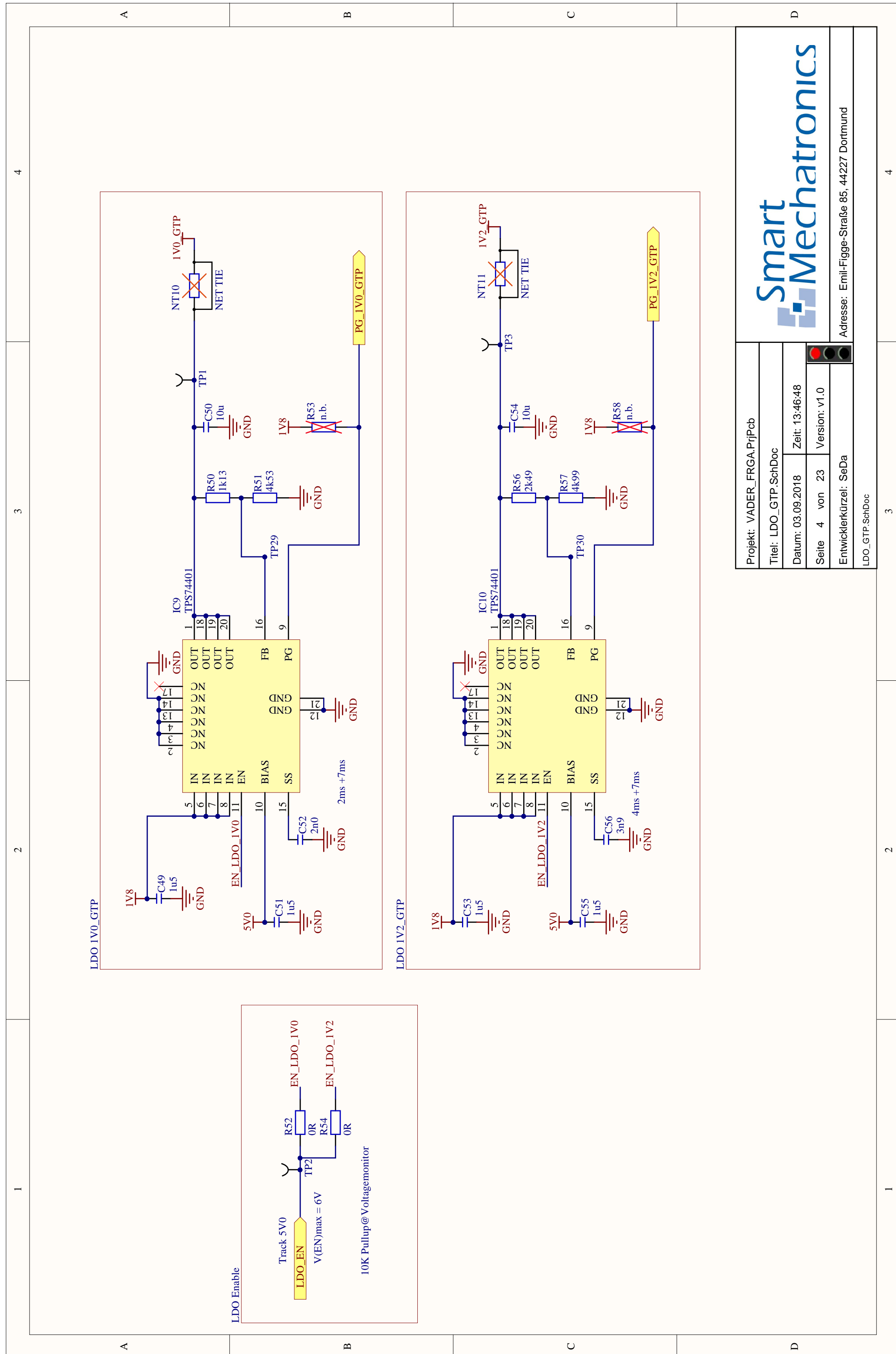
LED_DEBUG
LED_DEBUG.SchDoc



Projekt: VADER_FRGA.PrjPcb
Titel: VADER_FRGA.SchDoc
Datum: 03.09.2018 Zeit: 13:46:48
Seite 1 von 23 Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
VADER_FRGA.SchDoc


Input Protection
Supply 1V8
Supply DDR3 1V35
Supply 5V0
J8
103669-1
T6
FQD17P06
D19
SM6T36CA
R139
100k
12V0
1V8
1V35
5V0
GND
NET TIE
PG_1V8
PG_DDR3_1V35
PG_5V0
IC2
IC3
IC4
TPS82140
VIN
EN
SS/TR
VOUT
FB
PG
PAD
GND
R13
124k
R14
100k
R15
n.b.
R17
68k
R18
100k
R19
n.b.
R4
100k
R5
19k1
R23
n.b.
C22
10u
C23
22u
C24
6n2
C25
10u
C26
22u
C27
27n
C28
10u
C29
22u
C30
15n
3.1 ms
13.5 ms
7.5 ms
Smart Mechatronics
Projekt: VADER_FRGA.PrjPcb
Titel: BUCK_TPS82140.SchDoc
Datum: 03.09.2018
Zeit: 13:46:48
Seite 2 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
BUCK_TPS82140.SchDoc


Supply 3V3 1V0
IC1
LTC3636
Smart Mechatronics
Projekt: VADER_FRGA.PrjPcb
Titel: BUCK_LTC3636.SchDoc
Datum: 03.09.2018
Zeit: 13:46:48
Seite 3 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
BUCK_LTC3636.SchDoc



LDO 1V0_GTP
IC9
TPS74401
1V0_GTP
NT10
NET TIE
TP1
C50
10u
R50
1k13
R51
4k53
TP29
R53
n.b.
PG_1V0_GTP
C49
1u5
C51
1u5
C52
2n0
EN_LDO_1V0
2ms +7ms
LDO 1V2_GTP
IC10
TPS74401
1V2_GTP
NT11
NET TIE
TP3
C54
10u
R56
2k49
R57
4k99
TP30
R58
n.b.
PG_1V2_GTP
C53
1u5
C55
1u5
C56
3n9
EN_LDO_1V2
4ms +7ms
IN
EN
BIAS
SS
OUT
FB
PG
NC
GND
1V8
5V0
LDO Enable
LDO_EN
Track 5V0
V(EN)max = 6V
10K Pullup@Voltagemonitor
TP2
R52
0R
R54
0R
EN_LDO_1V0
EN_LDO_1V2
Smart Mechatronics
Projekt: VADER_FRGA.PrjPcb
Titel: LDO_GTP.SchDoc
Datum: 03.09.2018
Zeit: 13:46:48
Seite 4 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
LDO_GTP.SchDoc

Projekt: VADER_FRGA.PrjPcb

Titel: Voltage_Monitor.SchDoc

Datum: 03.09.2018 Zeit: 13:46:48

Seite 5 von 23 Version: v1.0

Entwicklerkürzel: SeDa

Adresse: Emil-Figge-Straße 85, 44227 Dortmund

Voltage_Monitor.SchDoc

Smart Mechatronics

Projekt: VADER_FRGA.PrjPcb

Titel: AnyBus.SchDoc

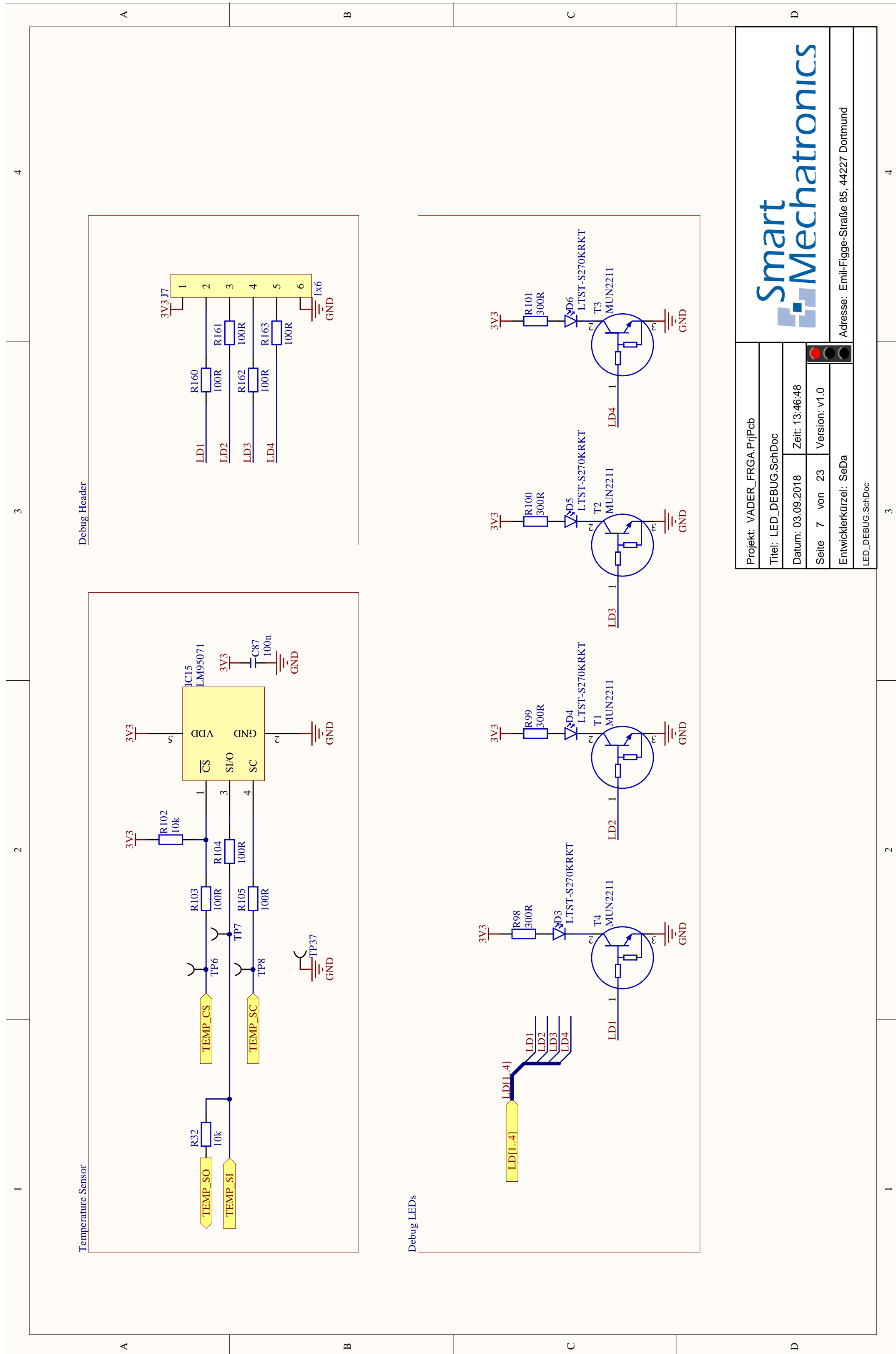
Datum: 03.09.2018 Zeit: 13:46:48

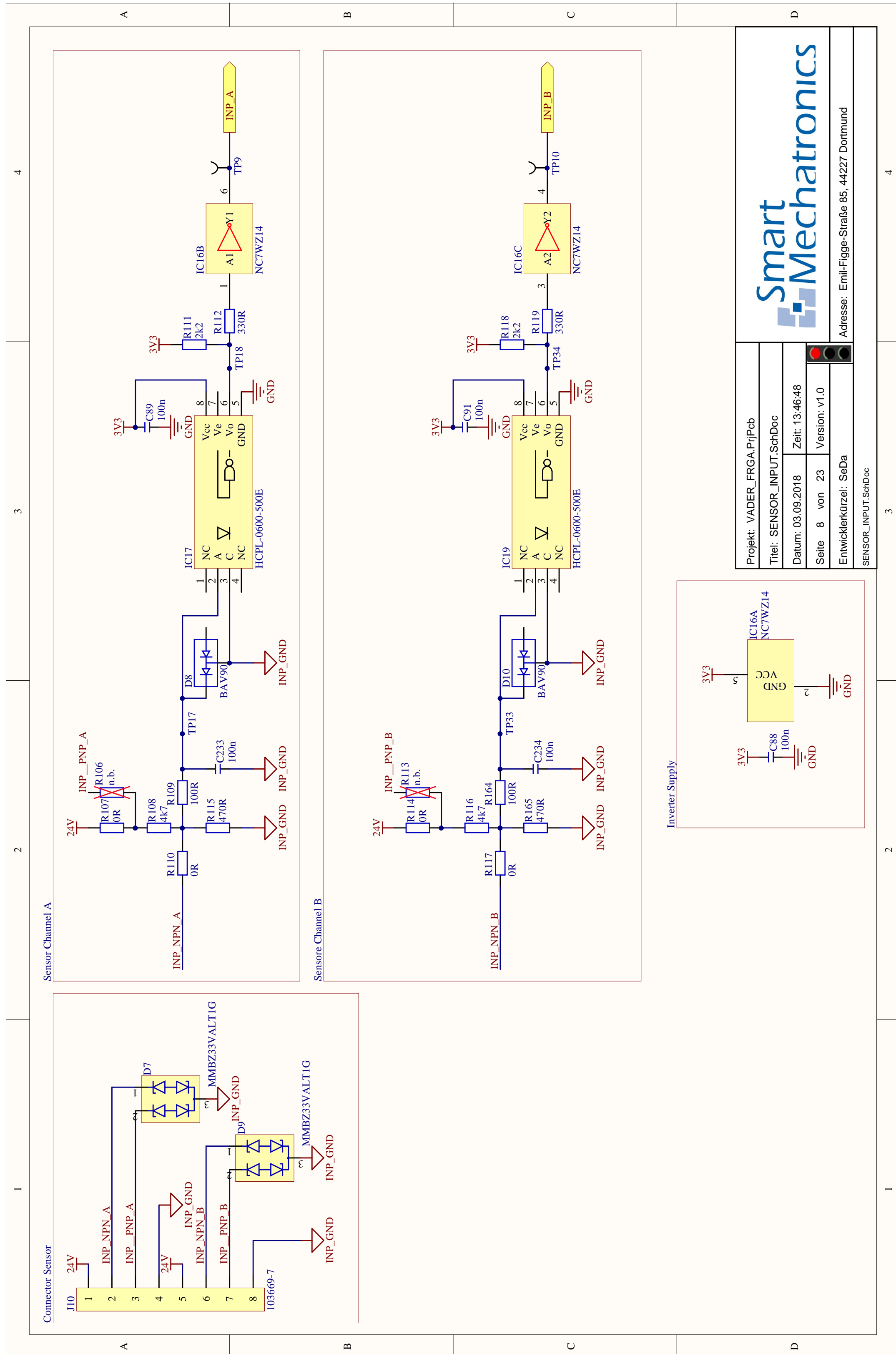
Seite 6 von 23 Version: v1.0

Entwicklerkürzel: SeDa

Adresse: Emil-Figge-Straße 85, 44227 Dortmund

AnyBus.SchDoc


Temperature Sensor
IC15
LM95071
VDD
GND
CS
SI/O
SC
3V3
GND
R102
10k
R103
100R
R104
100R
R105
100R
C87
100n
TP6
TP7
TP8
TP37
R32
10k
TEMP_CS
TEMP_SC
TEMP_SO
TEMP_SI
Debug Header
J7
1x6
R160
100R
R161
100R
R162
100R
R163
100R
LD1
LD2
LD3
LD4
Debug LEDs
LD[1..4]
R98
300R
R99
300R
R100
300R
R101
300R
D3
D4
D5
D6
LTST-S270KRKT
T1
T2
T3
T4
MUN2211
Projekt: VADER_FRGA.PrjPcb
Titel: LED_DEBUG.SchDoc
Datum: 03.09.2018
Zeit: 13:46:48
Seite 7 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
LED_DEBUG.SchDoc
Smart
Mechatronics


Sensor Channel A
Sensore Channel B
Connector Sensor
Inverter Supply
INP_A
INP_B
INP_NPN_A
INP_PNP_A
INP_NPN_B
INP_PNP_B
INP_GND
HCPL-0600-500E
NC7WZ14
MMBZ33VALT1G
BAV99
103669-7
Smart Mechatronics
Projekt: VADER_FRGA.PrjPcb
Titel: SENSOR_INPUT.SchDoc
Datum: 03.09.2018
Zeit: 13:46:48
Seite 8 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
SENSOR_INPUT.SchDoc

Smart Mechatronics

Incremental Connector

Incremental

Smart Mechatronics

Projekt: VADER_FRGA.PrjPcb

Titel: INCREMENTAL.SchDoc

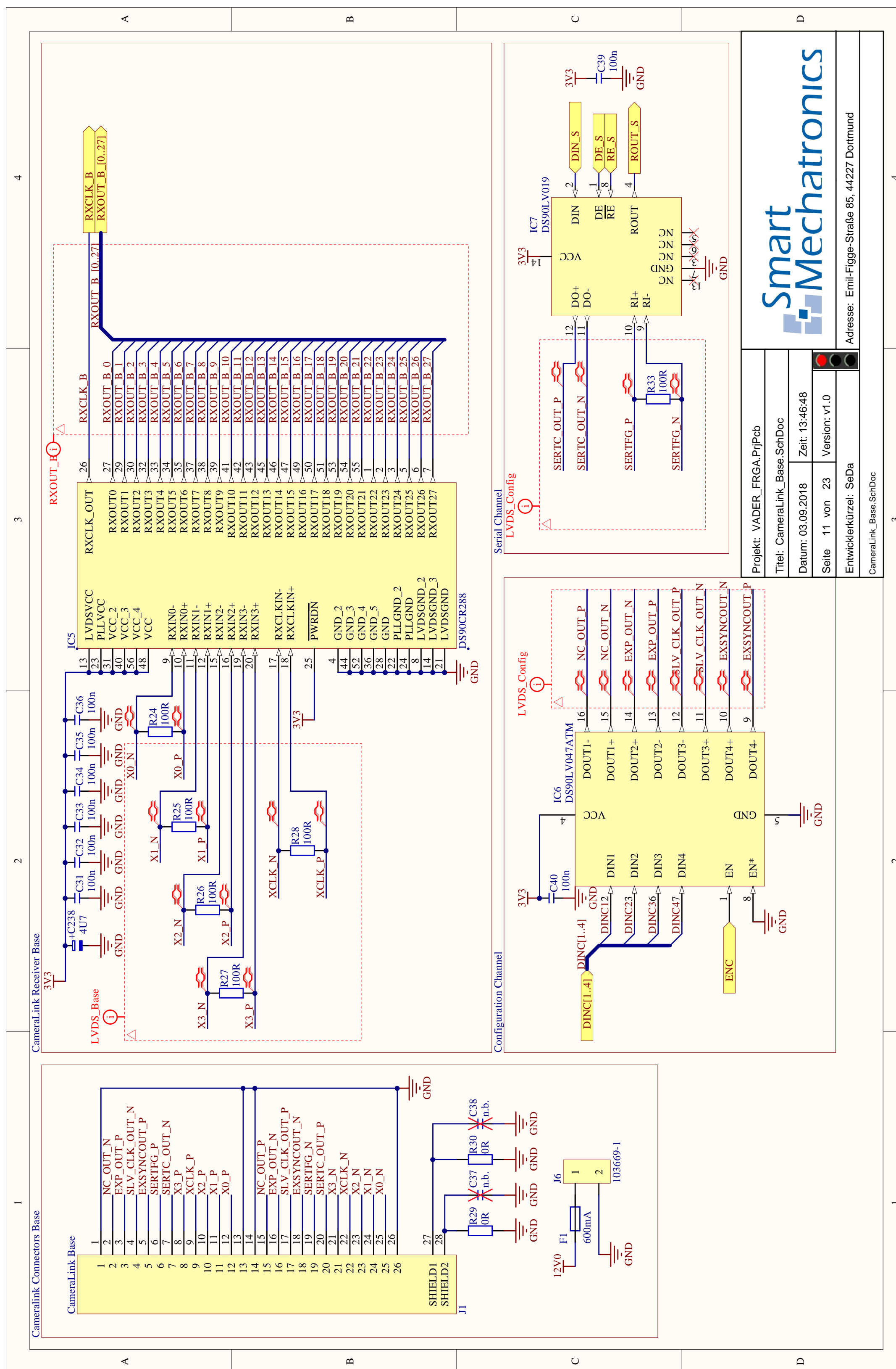
Datum: 03.09.2018 | Zeit: 13:46:48

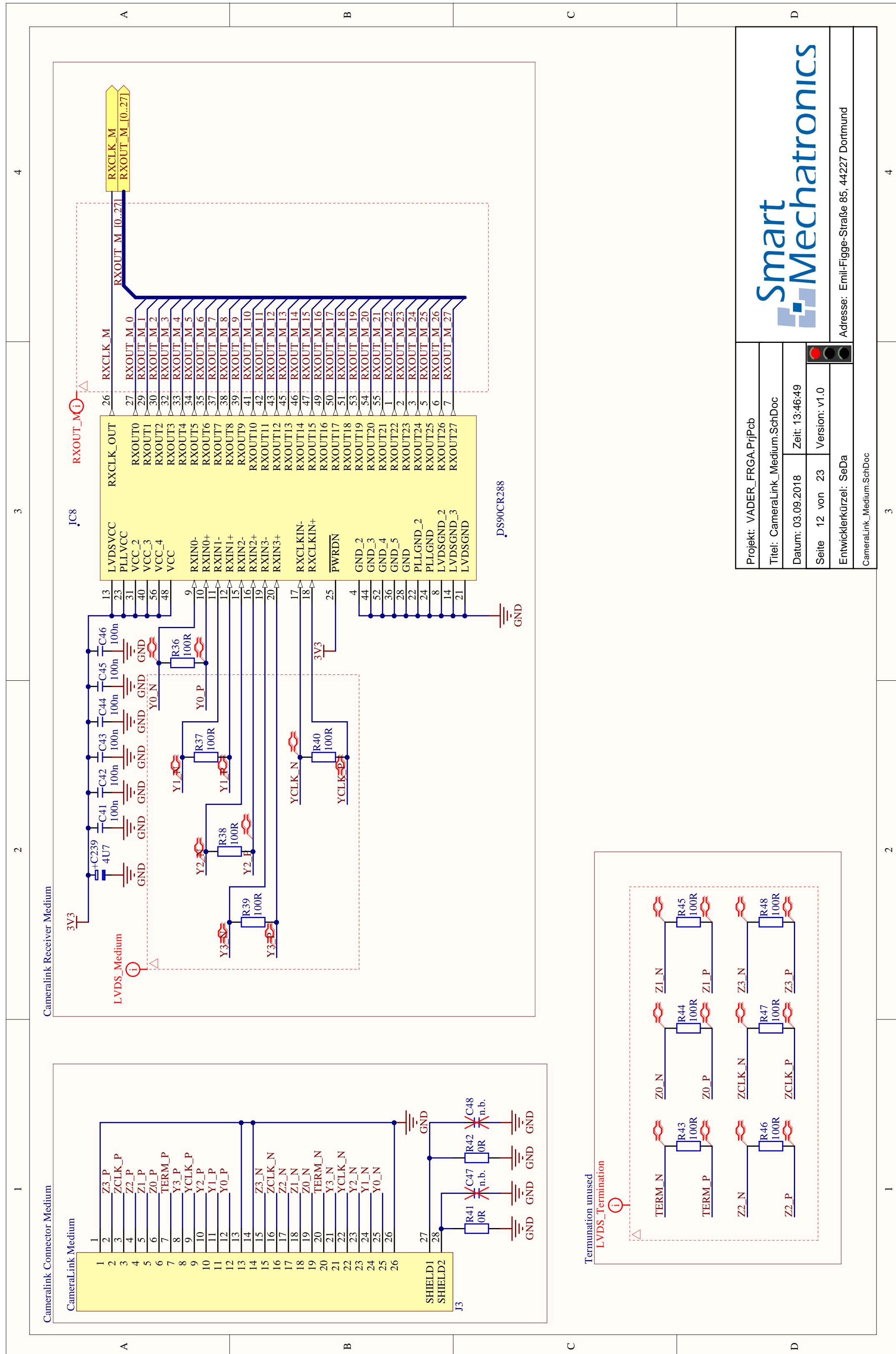
Seite 10 von 23 | Version: v1.0

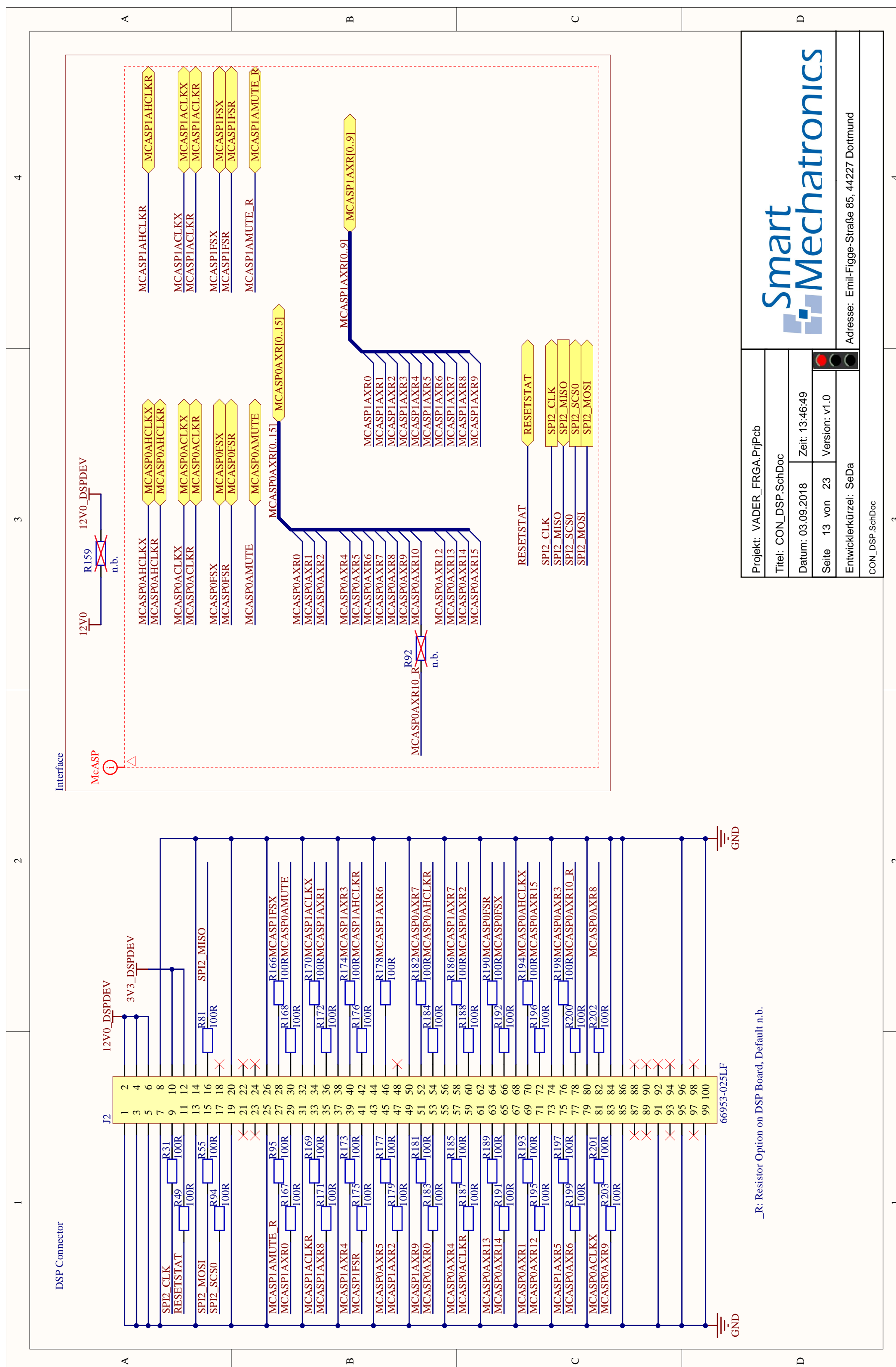
Entwicklerkürzel: SeDa

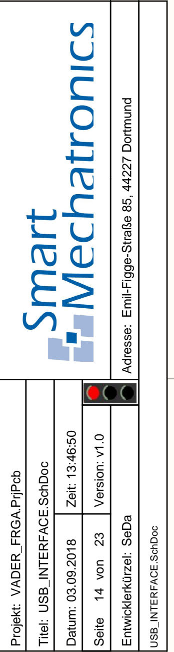
Adresse: Emil-Figge-Straße 85, 44227 Dortmund

INCREMENTAL.SchDoc




Cameralink Receiver Medium
Cameralink Connector Medium
CameraLink Medium
J3
IC8
DS90CR288
LVDS_Medium
RXOUT_M
RXCLK_M
RXOUT_M_[0..27]
Termination unused
LVDS_Termination
GND
3V3
Projekt: VADER_FRGA.PrjPcb
Titel: CameraLink_Medium.SchDoc
Datum: 03.09.2018
Zeit: 13:46:49
Seite 12 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
CameraLink_Medium.SchDoc
Smart Mechatronics


DSP Connector
Interface
McASP
_R: Resistor Option on DSP Board, Default n.b.
66953-025LF
GND
Smart Mechatronics
Projekt: VADER_FRGA.PrjPcb
Titel: CON_DSP.SchDoc
Datum: 03.09.2018
Zeit: 13:46:49
Seite 13 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
CON_DSP.SchDoc


Smart
Mechatronics

FPGA_BANKS1
FPGA_BANKS1.SchDoc
RXOUT_B_[0..27]
RXCLK_B
DE_S
RE_S
DIN_S
DINC[1..4]
ENC
ROUT_S
RXCLK_M
RXOUT_M_[0..27]
TEMP_SC
TEMP_CS
LD[1..4]
TEMP_SI
TEMP_SO
ANY_LED1B
ANY_LED2A
ANY_CE
ANY_MD0
ANY_OM2
ANY_OM0
ANY_LED2B
ANY_RX
ANY_LED1A
ANY_GIP0
ANY_OE
ANY_RW
ANY_GOP0
ANY_IRQ
ANY_MI1
ANY_GOP1
ANY_MI0
ANY_RESET
ANY_GIP1
ANY_OM1
ANY_TX

FPGA_BANKS2
FPGA_BANKS2.SchDoc
DDR3_BA[0..2]
DDR3_RESET
DDR3_CKE
DDR3_CK_P
DDR3_CS
DDR3_RAS
DDR3_CAS
DDR3_WE
DDR3_ODT
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_DQS1_P
DDR3_DQS1_N
DDR3_CK_N
DDR3_DM0
DDR3_DM1
DDR3_DQ[0..15]
DDR3_A[0..13]
SPI2_MOSI
SPI2_MISO
SPI2_SCS0
SPI2_CLK
RESETSTAT
MCASP1AMUTE_R
MCASP1FSX
MCASP1AHCLKR
MCASP1ACLKR
MCASP1FSR
MCASP1ACLKX
MCASP0AHCLKR
MCASP0ACLKX
MCASP0FSX
MCASP0FSR
MCASP0AMUTE
MCASP0ACLKR
MCASP0AHCLKX
MCASP0AXR[0..15]
MCASP1AXR[0..9]

DDR3
DDR3.SchDoc

FPGA_BANKS0
FPGA_BANKS0.SchDoc
xSPI_CS
xSPI_D1
xSPI_D2
xSPI_D3
xSPI_D0
FTDI_RXF
FTDI_TXE
FTDI_OE
FTDI_WR
FTDI_RD
FTDI_SIWUA
FTDI_D[0..7]
INC_A
INC_B
MON_INC
INP_A
INP_B
SSI_CLK
SSI_DTA

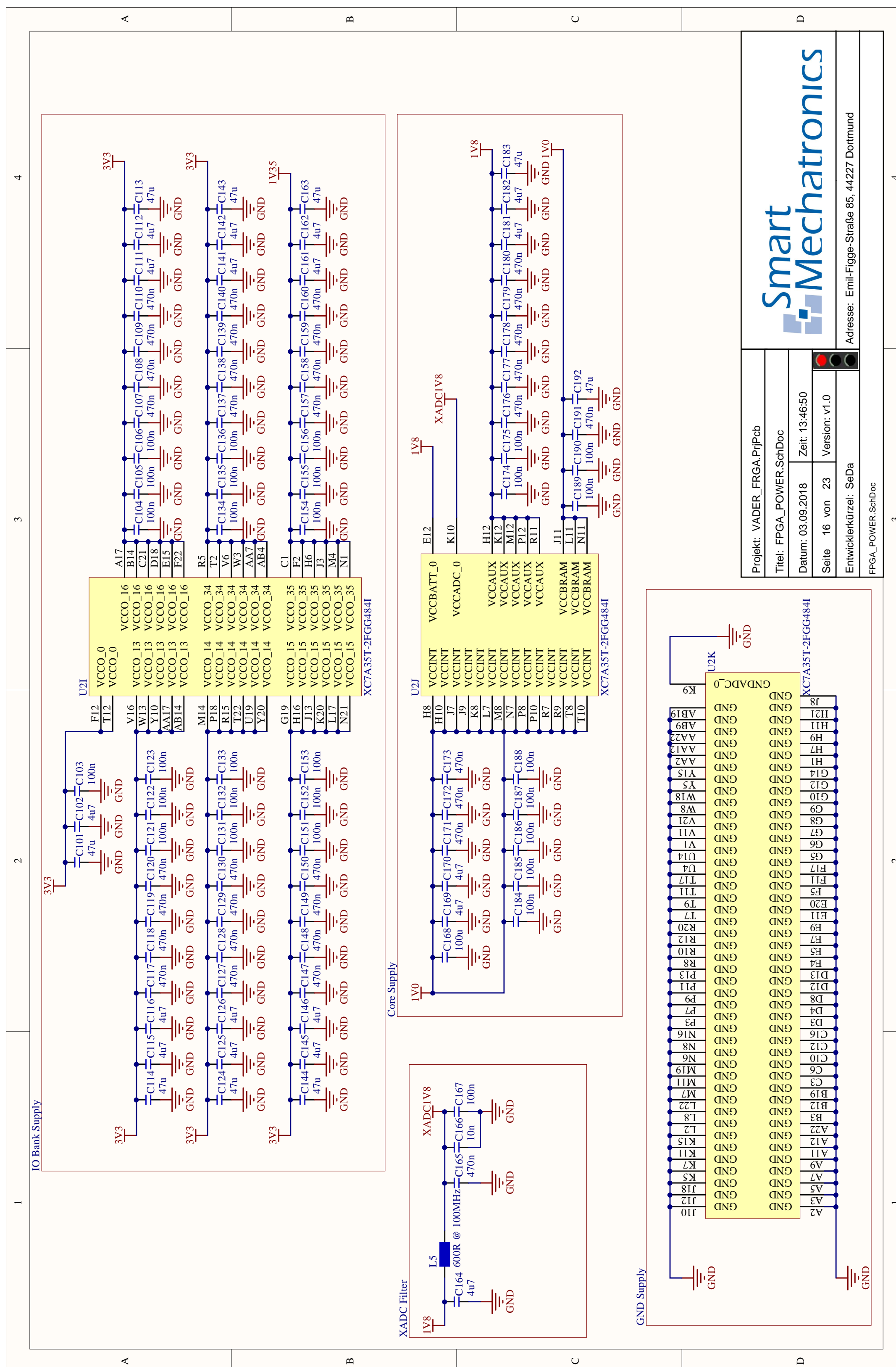
FPGA_CONFIG
FPGA_CONFIG.SchDoc
JTAG_TDI
JTAG_TDO
JTAG_TCK
JTAG_TMS
xSPI_CS
xSPI_D1
xSPI_D2
xSPI_D3
xSPI_D0
RESET

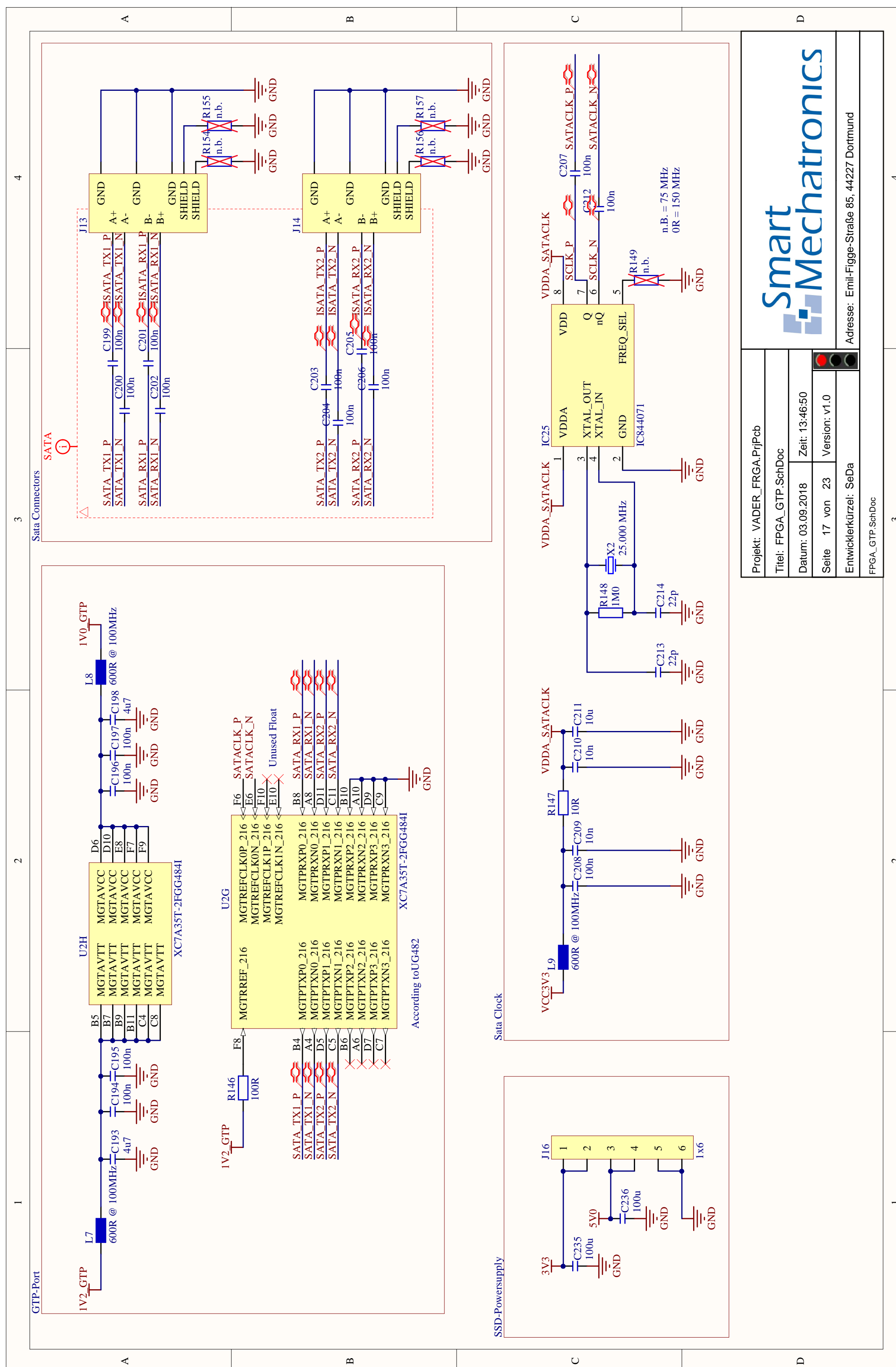
MCASPA0AMUTE
R180
n.b.
MASTER_RESET

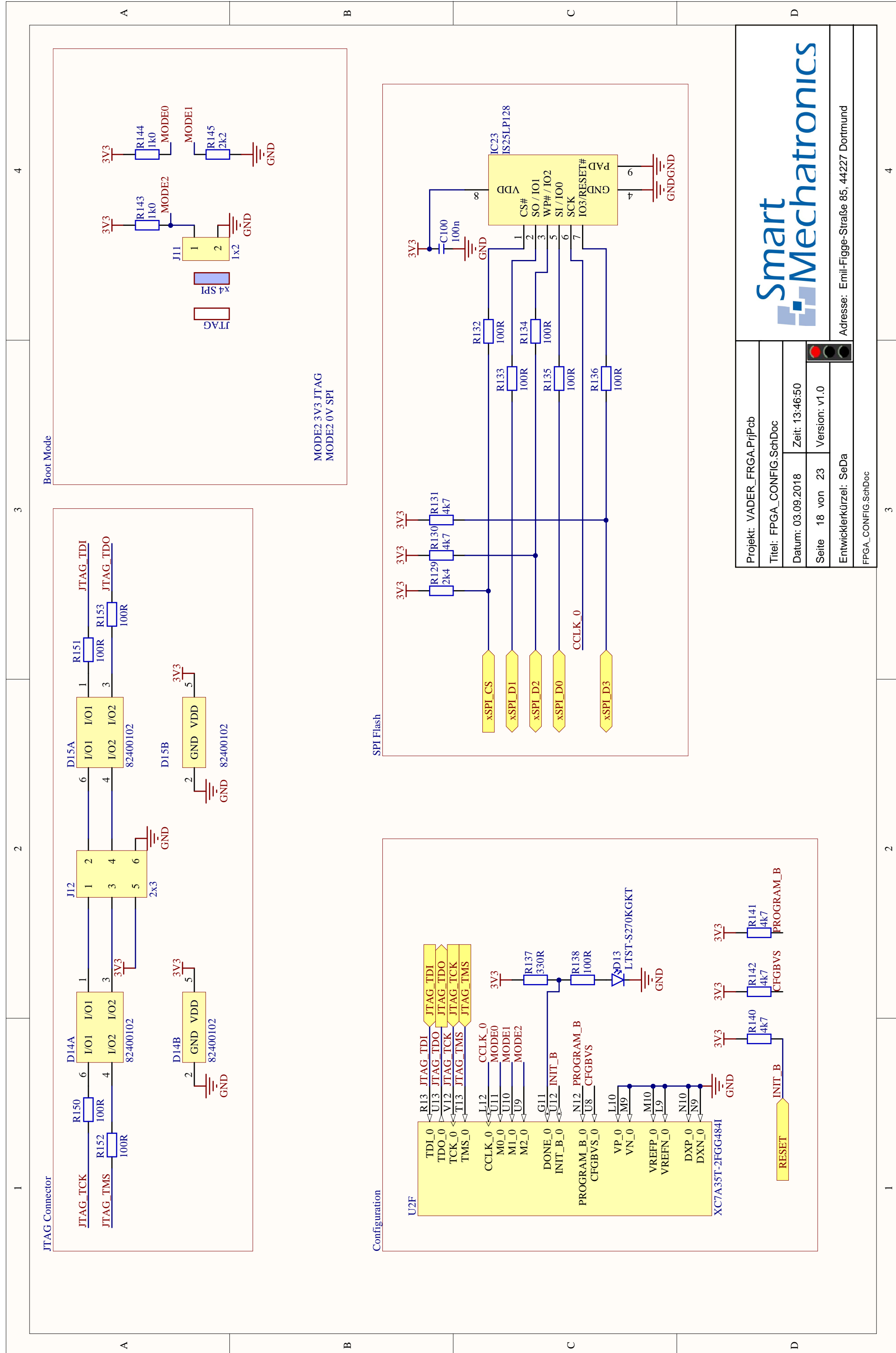
FPGA_POWER
FPGA_POWER.SchDoc

FPGA_GTP
FPGA_GTP.SchDoc

Projekt: VADER_FRGA.PrjPcb
Titel: FPGA_ALL.SchDoc
Datum: 03.09.2018 Zeit: 13:46:50
Seite 15 von 23 Version: v1.0
Entwicklerkürzel: SeDa
FPGA_ALL.SchDoc
Smart Mechatronics
Adresse: Emil-Figge-Straße 85, 44227 Dortmund


IO Bank Supply
Core Supply
XADC Filter
GND Supply
Smart Mechatronics
Projekt: VADER_FRGA.PrjPcb
Titel: FPGA_POWER.SchDoc
Datum: 03.09.2018
Zeit: 13:46:50
Seite 16 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
FPGA_POWER.SchDoc


Sata Connectors
GTP-Port
Sata Clock
SSD-Powersupply
Smart Mechatronics
Projekt: VADER_FRGA.PrjPcb
Titel: FPGA_GTP.SchDoc
Datum: 03.09.2018
Zeit: 13:46:50
Seite 17 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
FPGA_GTP.SchDoc


Boot Mode
JTAG Connector
SPI Flash
Configuration
MODE2 3V3 JTAG
MODE2 0V SPI
JTAG
x4 SPI
J11
1x2
J12
2x3
D14A
D14B
D15A
D15B
82400102
U2F
XC7A35T-2FGG484I
IC23
IS25LP128
C100
100n
D13
LTST-S270KGKT
xSPI_CS
xSPI_D1
xSPI_D2
xSPI_D0
xSPI_D3
RESET
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
CCLK_0
INIT_B
PROGRAM_B
CFGBVS
3V3
GND
Projekt: VADER_FRGA.PrjPcb
Titel: FPGA_CONFIG.SchDoc
Datum: 03.09.2018
Zeit: 13:46:50
Seite 18 von 23
Version: v1.0
Entwicklerkürzel: SeDa
FPGA_CONFIG.SchDoc
Smart Mechatronics
Adresse: Emil-Figge-Straße 85, 44227 Dortmund

Bank 14

U2A

BANK 14

XC7A35T-2FGG484I

3V3 R127 1k0

R128 n.b.

GND

FTDI_D[0..7]

NC

U2L

XC7A35T-2FGG484I

Smart Mechatronics

Projekt: VADER_FRGA.PrjPcb

Titel: FPGA_BANKS0.SchDoc

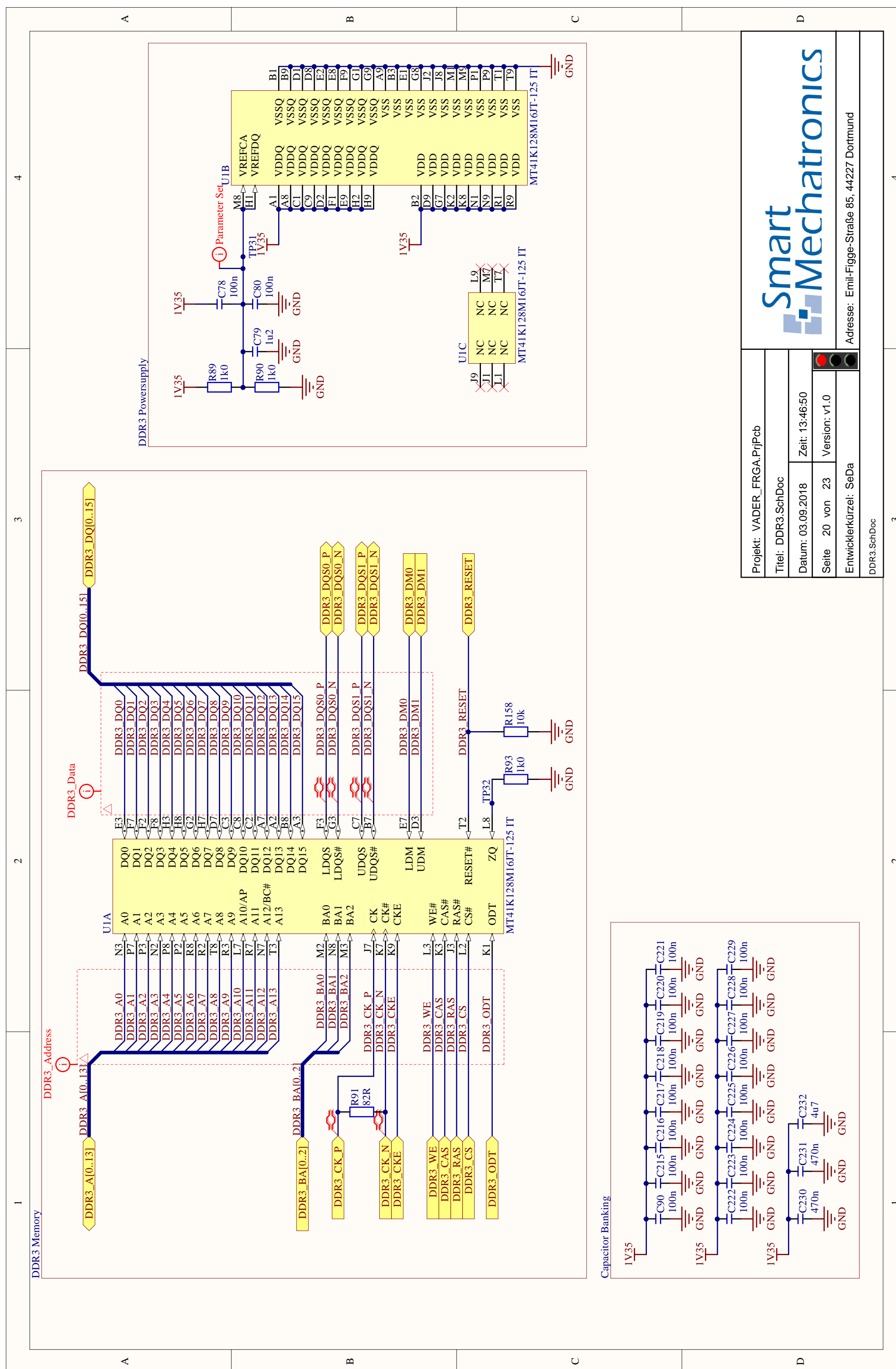
Datum: 03.09.2018 | Zeit: 13:46:50

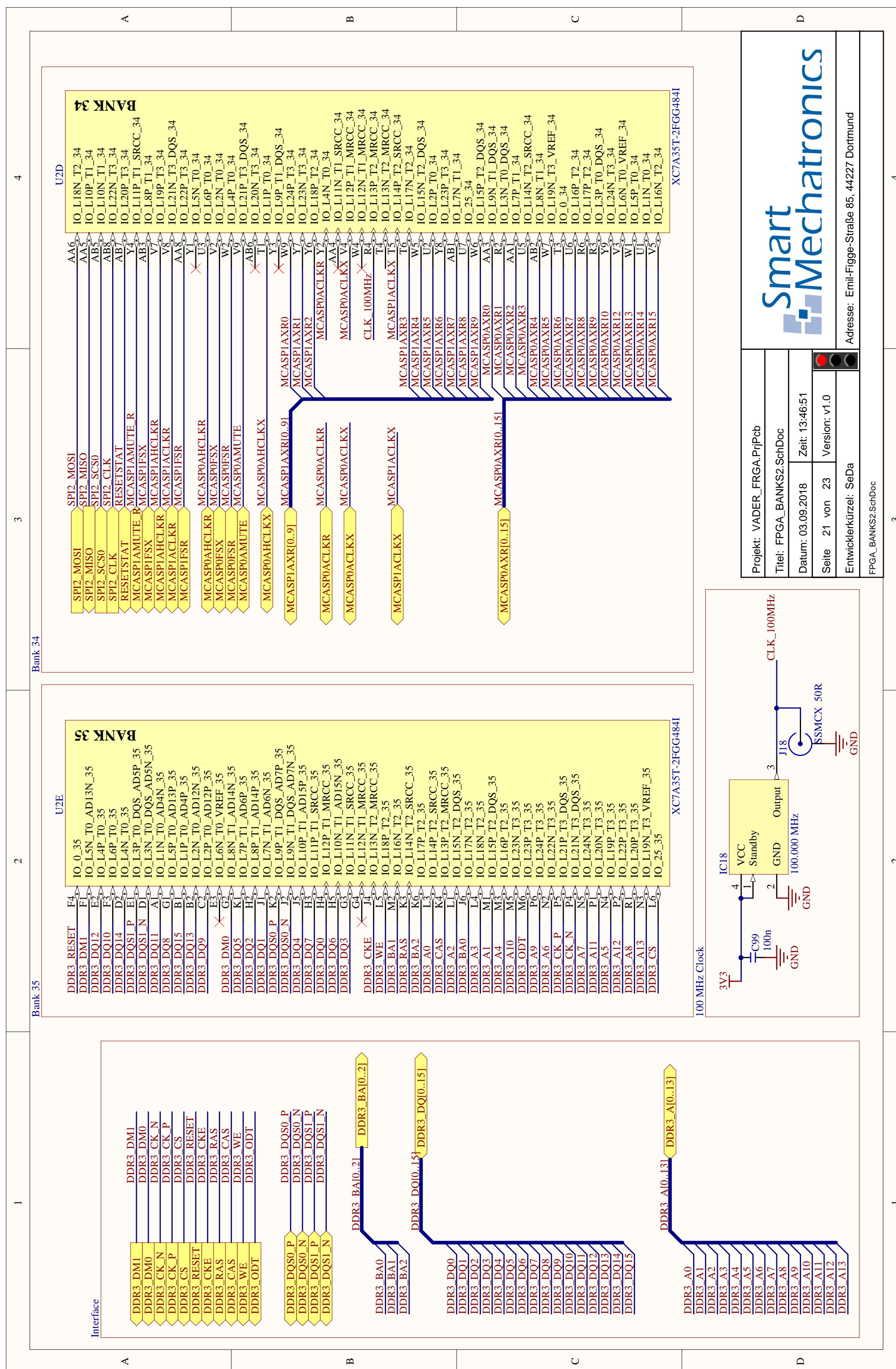
Seite 19 von 23 | Version: v1.0

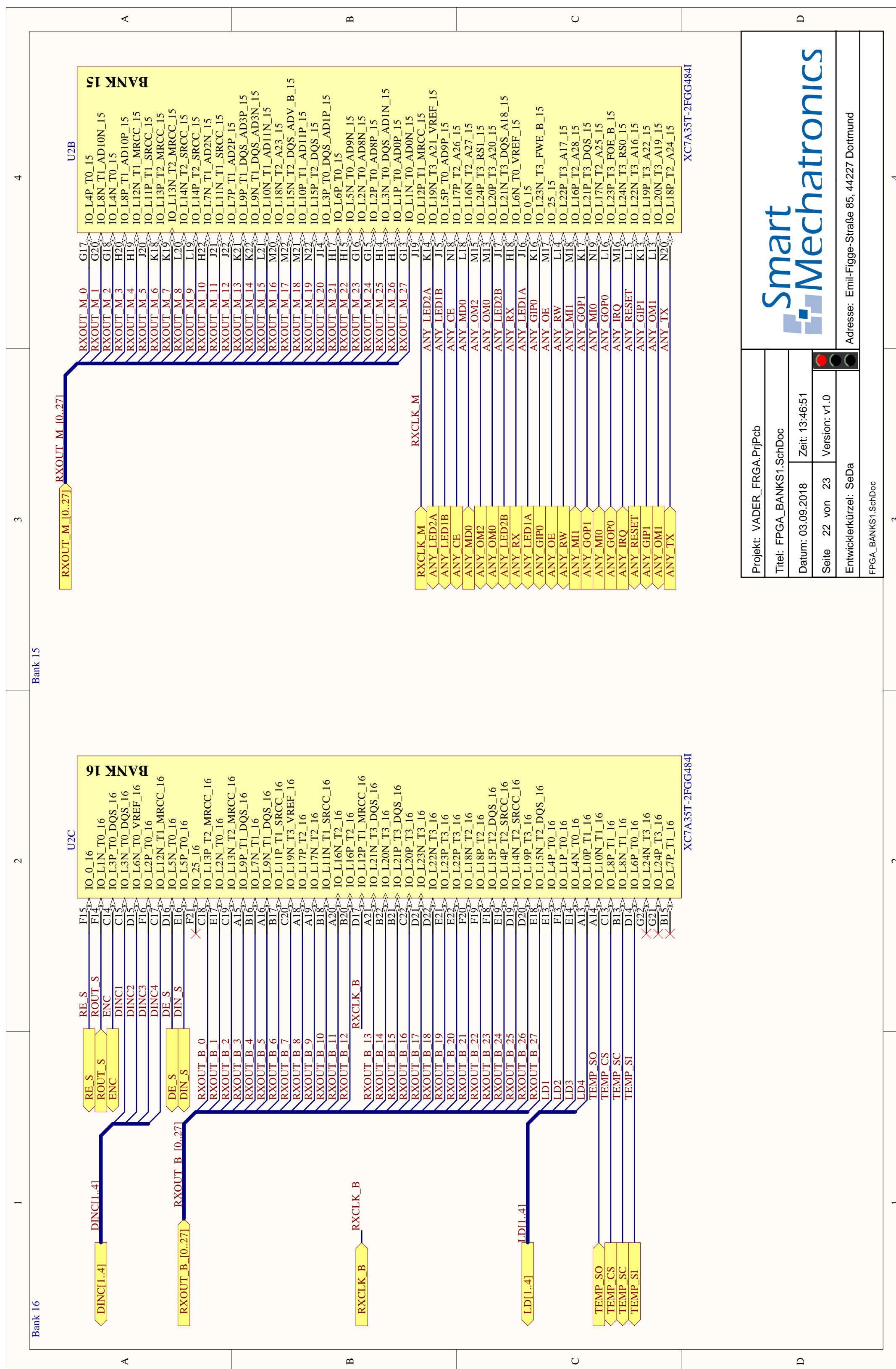
Entwicklerkürzel: SeDa

Adresse: Emil-Figge-Straße 85, 44227 Dortmund

FPGA_BANKS0.SchDoc


DDR3 Powersupply
DDR3 Memory
Capacitor Banking
DDR3_Address
DDR3_Data
MT41K128M16JT-125 IT
Smart Mechatronics
Projekt: VADER_FRGA.PrjPcb
Titel: DDR3.SchDoc
Datum: 03.09.2018
Zeit: 13:46:50
Seite 20 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
DDR3.SchDoc


Bank 35
BANK 35
U2E
XC7A35T-2FGG484I
Bank 34
BANK 34
U2D
XC7A35T-2FGG484I
Interface
100 MHz Clock
IC18
100.000 MHz
SSMCX_50R
CLK_100MHz
3V3
GND
Projekt: VADER_FRGA.PrjPcb
Titel: FPGA_BANKS2.SchDoc
Datum: 03.09.2018
Zeit: 13:46:51
Seite 21 von 23
Version: v1.0
Entwicklerkürzel: SeDa
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
Smart Mechatronics
FPGA_BANKS2.SchDoc



U2B
BANK 15
XC7A35T-2FGG484I
U2C
BANK 16
XC7A35T-2FGG484I
Bank 15
Bank 16
RXOUT_M_[0..27]
RXCLK_M
RXOUT_B_[0..27]
RXCLK_B
DINC[1..4]
LD[1..4]
RE_S
ROUT_S
ENC
DE_S
DIN_S
TEMP_SO
TEMP_CS
TEMP_SC
TEMP_SI
Projekt: VADER_FRGA.PrjPcb
Titel: FPGA_BANKS1.SchDoc
Datum: 03.09.2018
Zeit: 13:46:51
Seite 22 von 23
Version: v1.0
Entwicklerkürzel: SeDa
FPGA_BANKS1.SchDoc
Adresse: Emil-Figge-Straße 85, 44227 Dortmund
Smart Mechatronics